IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received May 13, 2019, accepted June 30, 2019, date of publication July 15, 2019, date of current version August 1, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2928896

Power Integrity Coanalysis Methodology for Multi-Domain High-Speed Memory Systems

SEUNGWON KIM[1], (Student Member, IEEE), KI JIN HAN[2], (Senior Member, IEEE), YOUNGMIN KIM[3], (Member, IEEE), AND SEOKHYEONG KANG[4], (Member, IEEE)

[1]Department of Electrical Engineering, Ulsan National Institute of Science and Technology, Ulsan 44919, South Korea
[2]Division of Electronics and Electrical Engineering, Dongguk University, Seoul 04620, South Korea
[3]School of Electronic and Electrical Engineering, Hongik University, Seoul 04066, South Korea
[4]Department of Electrical Engineering, Pohang University of Science and Technology, Pohang 37673, South Korea

Corresponding author: Seokhyeong Kang (shkang@postech.ac.kr)

This work was supported in part by the Creative Materials Discovery Program through the National Research Foundation of Korea (NRF), Ministry of Science and ICT, under Grant 2017M3D1A1040828, in part by the Nano-Material Technology Development Program through the National Research Foundation of Korea (NRF), Ministry of Science and ICT, under Grant 2016M3A7B4909943, and in part by the ITRC (Information Technology Research Center) support program supervised by the IITP (Institute for Information and communications Technology Promotion), MSIT (Ministry of Science and ICT), South Korea, under Grant IITP-2019-2016-0-00309-002.

ABSTRACT With the increasing demand for state-of-the-art technologies, such as wearable devices and the Internet of things (IoT), power integrity has emerged as a major concern for high-speed, low-power interfaces that are used as mobile platforms. By using case-specific design models in a high-speed memory system, only a limited analysis of the effects of parametric variations can be performed in complex design problems, such as adjacent voltage domain coupling at high frequencies. Moreover, a conventional industrial method can be simulated only after completing the design layout; therefore, a number of iterative back-annotation processes are required for signoff; this delays the time to market. In this paper, we propose a power integrity coanalysis methodology for multiple power domains in high-frequency memory systems. Our proposed methodology can analyze the tendencies in power integrity by using parametric methods, such as parameter sweeping and Monte Carlo simulations. Our experiments prove that our proposed methodology can predict similar peak-to-peak ripple voltages that are comparable with the realistic simulations of low-power double data rate four interfaces.

INDEX TERMS Power integrity (PI), multi-domain coupling, high-speed memory, power delivery system, power distribution network (PDN), chip-package-PCB coanalysis, analysis methodology, low power double data rate four (LPDDR4).

I. INTRODUCTION

Recently, the data rate and clock speed of high-speed I/O interfaces, such as mobile memory, have increased beyond the gigabit-per-second level. Circuits and packaging have also become highly integrated. However, although target performances have been met, certain undesirable effects, such as mismatch and crosstalk, have also occurred in systems. In addition, physical limitations reveal low power efficiency with increasing input/output (I/O) bandwidth between the central processing unit and memory [2]. Therefore, we need to maximize the performance of the electrical links in a printed circuit board (PCB) and the package structure in high-speed signal transmission conditions.

The packaging structure causes static and dynamic power losses. In addition, the memory system requires additional on-chip power consumption to ensure signal integrity, such as on-die termination and an equalizer. Therefore, in a high-speed memory system that requires a low-power mobile device, the package structure needs to minimize the power loss to ensure power integrity (PI). It is important to analyze the effect of the decoupling capacitors on the dynamic power loss because the power distribution network (PDN) in the system also causes frequency-dependent IR drops [3]. In the state-of-the-art mobile and wearable devices, we need to consider coupling the separate power domains as well. The current low-power memory systems apply multiple power domains to deliver power with adequate supply voltage (VDD) levels. Each power domain has its own noise and switching activity [4]. For example, the high-speed low-power double data rate four (LPDDR4) memory has three power domains: VDD1 and VDD2 for the core and VDDQ for the I/O buffers [5]. However, previous multi-domain studies have focused on case-specific design

The associate editor coordinating the review of this manuscript and approving it for publication was Gian Domenico Licciardo.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see http://creativecommons.org/licenses/by/4.0/

analysis or the lack of coanalysis on the package in the system [6]–[8].

A prediction of power integrity in high-frequency systems is difficult; therefore, to overcome the signoff constraint and improve results, the industry has designed chip-package-PCBs by numerous back-annotations instead of efficient codesigns. It is time-consuming to simulate the full layout of the memory system using a realistic package and PCB model with electronic design automation (EDA) tools; a complete layout is also required [6], [9]. Therefore, to reduce the number of iterations in the design process, it is necessary to analyze the effect of the design variables that constitute the memory system on the PI. However, in previous case-specific design models [7], [8], it was difficult to construct a new model when the memory system variables changed. In the simplified models at the system level [6], it was difficult to model the parameters required for a practical package design for the memory system. Therefore, if the practical extracted parameters and the numerical model are compatible with each other in one analysis methodology, it is possible to have fast and massive parametric simulations at the proper level of accuracy.

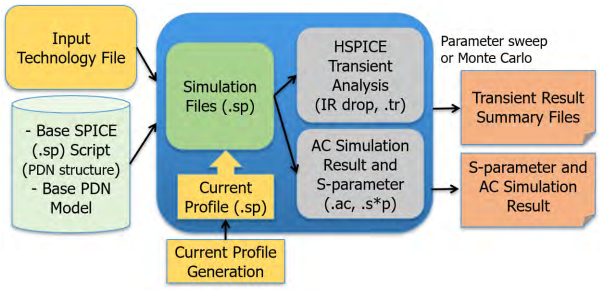

FIGURE 1. Process of our proposed PI coanalysis methodology.

In accordance with the recent design trends, we propose a PI design methodology that considers the effects of the electrical and structural parameters on the multi-voltage domain PCB-package-chip system (see Figure 1). For PI analysis, we construct a parametric link model that can quickly and accurately predict electrical performances according to the various design variables of a high-speed link. In addition, we develop a statistical analysis of the performance data derived from the link model that provides design guidelines. Thus, we propose a parametric link simulation environment that considers the electrical characteristics of the on-chip high-frequency switching current, and the physical effects of the package-PCB in multiple power domains. We verify our proposed coanalysis methodology by using the simulated program with integrated circuit emphasis (SPICE) results under the Joint Electron Device Engineering Council (JEDEC) LPDDR4 environment with an industrial results. We derive the results of the transient and AC simulation by using the proposed model based on the parameters that reflect the characteristics of the power delivery system (PDS).

The main contributions of our work are as follows:

- We propose a coanalysis methodology for PI, and verify it by using a full layout SPICE simulation under the JEDEC LPDDR4 environment.
- We also propose a pseudo-random current profile that characterizes realistic on-chip current profiles with that the desired design constraints.
- We analyze the effect of (1) the domain coupling in the package, (2) the on-chip decoupling capacitor, and (3) the input noise for power integrity with sweep or Monte Carlo simulations of the design parameters.
- Our proposed PI coanalysis methodology can perform fast and massive simulations based on the various design parameters of the PDS.

The remainder of this paper is organized as follows. Section II describes our PI coanalysis methodology, which consists of the chip-package-PCB, the supply power source, and the current profile generation method. Section III presents a procedure of proposed methodology. Our verification results and the analyses of the case simulations are described in Section IV. Section V concludes our work.

II. POWER DELIVERY SYSTEM ANALYSIS MODEL

A common method for constructing a memory system is the traditional discrete isolated-chip packaging for disposing a system-on-a-chip (SoC) and memory in two dimensions. However, in a mobile system that requires low power and high integration density, the *package-on-package* (PoP) stacking method with short vertical interconnection is the preferred application [10], [11]. Therefore, we implement the PoP method to model a PDS between the SoC and memory chip as shown in Figure 2.

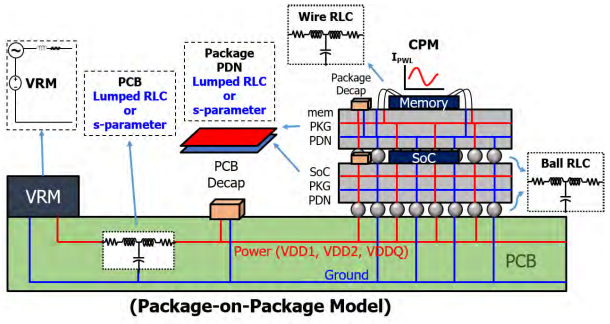

FIGURE 2. Overview of the PDS for a PoP model.

In the PDS model, the power is transferred from the voltage regulator module (VRM) to the memory chip through a PCB board, an SoC package, and a memory package. The PCB and each package include decoupling capacitors to reduce the frequency-dependent noise; they also include a multi-domain PDN model. We assumed wire bonding between the package and the chip. We modeled the on-chip with the switching current by using the memory operation as the redistribution layer (RDL) and the current profile. The following subsections describe the details of each component of the PDS model.

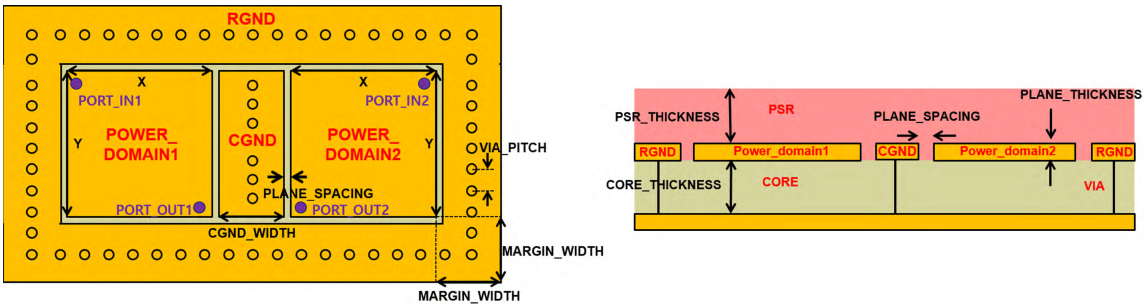

FIGURE 3. Structure and parameters of a simple multi-domain PDN. Top view (left) and side view (right).

A. MULTI-DOMAIN POWER DISTRIBUTION NETWORK

There are various methods for modeling a package-level PDN in a general single-power domain based on the impedance calculation [12] and the extraction from the physical structure and application to the equivalent resistor-inductor-capacitor (hereinafter RLC) model [13]–[15]. To analyze how the changes of the PDN structure affect the power domain coupling, we use a modeling method that extracts the scattering parameters (S-parameters) based on the physical structure. To prevent coupling between the power domains, a ground plane is placed between them in general. We use a PDN structure with two power domains as shown in Figure 3. This PDN structure has two power domains and ground planes. The two power domains are surrounded by a ring ground and placed separately next to the center ground plane. Each ground plane is connected to the bottom ground plane by vias. The design parameters are described in Figure 3 and Table 1.[1] This PDN structure is electrically small and simple compared with the realistic PDN geometry, and the location of the port in the same power plane is not dominant. Therefore, we choose the input/output ports of the two domains, as shown in Figure 3 (left). We mainly consider three design parameters to analyze the domain coupling effect. First, we change the existence of the central ground (hereinafter CGND) and the ring ground (hereinafter RGND). Second, we vary the width of the edges around the power domain planes (MARGIN_WIDTH); the other dimensions are keep fixed.

B. INPUT POWER SOURCE

The VRM consists of a DC-DC converter and a feedback control circuit that supplies the reference voltage required by the system for the output stage. The VRM is basically a nonlinear system. However, when the nonlinear model is implemented in the power transfer model, the simulation runtime becomes long, and it becomes difficult to set the parameters that determine the characteristics of each element in the VRM. Therefore, when the power transfer model is constructed to analyze the power integrity, the VRM is simplified into a linear model. The buck switching regulator is a widely used nonlinear VRM model [17], which we simplify into a linear model for a *SPICE* simulation. For the VRM, a four-element linear model can be used, as shown in Figure 4(a). However, the four-element model is a case-dependent model, and L_{slew} and R_{flat} need to be extracted from the nonlinear model; therefore, it is difficult to determine the value of the elements at the stage in which the PCB impedance has not yet been determined [18]. Our aim is to analyze the PDS model and treat the VRM as an input source. We use simplified two-element models instead of predicting the PCB impedance in advance, as shown in Figure 4(b).

Based on the two-element linear model, we add the sinusoidal noise source and the VDD offset. L_{out} is the inductance value of the cable between the VRM and the system board; it affects the maximum effective frequency. R_0 represents the resistance between the VRM sense point and the actual load. The R_0 of VRM can be calculated as follows:

$$R_0 = \rho \frac{l}{A} \tag{1}$$

TABLE 1. Modeling parameters and dimensions of multi-domain PDN. The value is the parameter value that is the reference of the PDN structure to be used in the simulation.

Name	Description	Value
PAD_PITCH	Interval length of ports	$1500\mu m$
PLANE_SPACING	Interval length of planes in a same layer	$200\mu m$
PLANE_THICKNESS	Thickness of the power domain planes and ground planes	$200\mu m$
POWER_DOMAIN 1_X,Y	The x-y-dimensions of the power domain 1 plane	$4500\mu m$
POWER_DOMAIN 2_X,Y	The x-y-dimension of the power domain 2 plane	$4500\mu m$
CGND	Central ground plane	1 (exists) or 0 (not)
CGND_X	The x dimension of the central ground plane	$2000\mu m$
CGND_Y	The y dimension of the central ground plane	$4500\mu m$
RGND	Ring ground plane	1 (exists) or 0 (not)
MARGIN_WIDTH	Width of the extra part outside power domain planes in the edge of PDN	Varying
CORE	Dielectric	ϵ_r = 3.9, tanδ = 0.02
CORE_THICKNESS	Thickness of dielectric	$400\mu m$
PSR	Prepreg	ϵ_r = 3.9, tanδ = 0.029
PSR_THICKNESS	Thickness of prepreg	$200\mu m$
VIA	Ground vias	d = $300\mu m$
VIA_PITCH	Interval length of ground vias	$500\mu m$

[1]The PDN model for multi-power domains is referred to in the preliminary analysis [16].

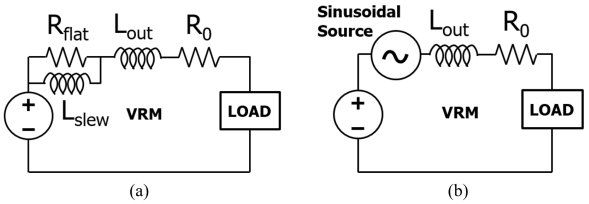

FIGURE 4. (a) Four-element linear VRM model and (b) the proposed two-element linear input power source model with a sinusoidal source as the noise.

TABLE 2. Sinusoidal source parameters.

Sinusoidal parameter	Units
V_0 - offset voltage	volt
V_a - peak amplitude of voltage	volt
$Freq$ - frequency	hertz
T_d - delay time	second
D_f - damping factor	1/second

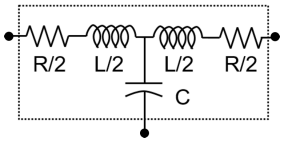

FIGURE 5. Lumped RLC T-model.

where ρ is the resistivity (assuming copper is used in this model); A is the cross-sectional area of the die; and l is the maximum path length.

We model the input noise itself as a sinusoidal source to make it easier to use in EDA analysis. The noise ripple and the VRM frequency is set in the sinusoidal source, and the DC voltage level is determined by setting the VDD offset. In this way, the PDS input can be adjusted as an environment similar to the VDD source output from the actual VRM. The sinusoidal source can be formulated as follows:

$$V_0 + V_a \cdot sin\left[2\pi\left[Freq \cdot (time - T_d) + \frac{Phase}{2\pi}\right]\right] \cdot e^{-(time-T_d)\cdot D_f} \quad (2)$$

The parameters are shown in Table 2.

C. ON-CHIP MODELING

1) ON-CHIP REDISTRIBUTION LAYER

The On-chip RDL is used to route the wire from the bonding pads to the bump pads without changing the position of the I/O pads. The RDL is placed on the top metal layer of the die. In our PDS analysis model, we use a simple lumped RLC T-model because the capacitance and inductance of the RDL are relatively small in the overall system (see Figure 5).[2] The T-model is electrically bi-directional, which is closer to the realistic PDN model and has higher accuracy than the RLC model in AC analysis [19]. The RDL model is connected to the memory package wire and the on-chip pad model that consists of a lumped resistor and a capacitor.

We use a pseudo-random current profile that reflected the behavior of the real current in the chip's characteristics because it is difficult to implement a realistic signal channel or use an industrial current profile.

2) ON-CHIP CURRENT PROFILE GENERATION

In general, to reduce the problems faced during simulation and runtime, PI analysis is performed by SPICE simulation using the chip power model (CPM) [20] with the input/output buffer information specification (IBIS) model [21] in the PDS instead of the realistic channel model [22]. The CPM contains information about the on-chip, and it is easy to use in a package and with the PCB design. However, it is difficult to coanalyze between the on-chip elements and the package design elements by using the CPM. For instance, the CPM already includes the RDL, the on-chip capacitance, and the metal resistance and inductance. Therefore, it has less flexibility in design simulation from the perspective of the package and the PCB designer.

On the other hand, a current profile is generated by referring to the target impedance of the PDS. Kim *et al.* [23] assumed that the maximum IC switching current of memory had a simple triangular shape for the peak current. However, this is an optimistic method because it is difficult to predict the PI due to parasitic capacitance and the inductance at high frequency in real PDSs. Chen *et al.* [24] implemented a memory controller hub and dynamic random-access memory modules to generate a current profile. However, creating a current profile through a memory module design is also difficult for the same reason as that for CPM. In addition, the current profile of the commercial memory is not available to the public. Therefore, in our methodology, we propose a pseudo-random current profile generation.

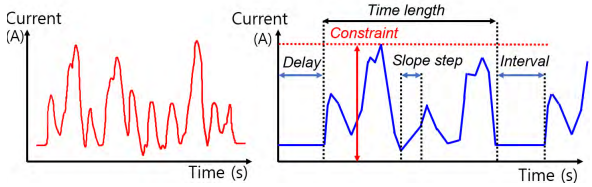

FIGURE 6. (a) Real on-chip current profile on the pad of VDDQ. (b) Overview of the characterized pseudo-random current profile parameters.

We first define the parameters that characterized the real on-chip current profile. Figure 6(a) shows the real on-chip current profile of VDDQ measured on the pad of the memory die. The characterized parameters to simulate the realistic operation are shown in Figure 6(b). We set the parameters so that they had a strong influence on the power transfer characteristics during realistic operations to achieve a current demand similar to a real memory operating environment. We take the min/max current constraint and the min/max *slope_step* value as the input parameters. In addition,

[2]Note that the lumped RLC value is obtained from the real RDL layout, and the resistance value significantly affects the static IR drop of the VDD as compared with the capacitance and inductance.

we generate a randomized piecewise linear waveform to satisfy the input condition. The *slope_step* determines the time between the changes in the current slope (di/dt) as one step. A random current value between the min/max *current constraint* is arbitrarily set for each *slope_step*. Then, the waveform is generated by increasing or decreasing based on the random current value while satisfying constraint. The *delay* parameter is the initial delay time in which the current profile starts. The *interval* represents the time taken to repeat the current generated for memory operations, and the *time_length* is the period of the repeated current profile excluding the interval. Note that the above parameters are not intended to exactly imitate the realistic waveforms; however, they are intended to facilitate analysis through parametric simulation by characterizing factors that affect the PI.

D. DECOUPLING CAPACITOR, WIRE AND BALL MODELING

A real decoupling capacitor has equivalent series inductance (ESL) and equivalent series resistance (ESR). As shown in Figure 2, the decoupling capacitors are connected to the PCB, the SoC package, and the memory package. In addition, we connect the decoupling capacitors with ESL and ESR.

We connect the wires and balls to the VRM, the package, the PCB, and the load by using the simple RLC model as shown in Figure 5. This RLC model is applicable when the length of the interconnect is electrically short, for example, in a ball structure. When the length of the wire exceeds 1/10th of the wavelength at the maximum modeling frequency (i.e., the knee frequency), the accuracy of the first-stage RLC model decreases. Therefore, we need to design the RLC model as a multistage series RLC network.

In the RLC model of the wire and ball, the value of the AC resistance (R) is calculated using the following equation [25]:

$$R \approx \frac{L\rho}{\pi(D-\delta)\delta}, \quad D >> \delta, \tag{3}$$

where δ is the skin depth, which is calculated as

$$\delta = \sqrt{\frac{2\rho}{\omega\mu_\gamma\mu_0}}, \tag{4}$$

where ρ represents the resistivity of the conductor; ω is the angular frequency; μ_γ is the relative magnetic permeability of the conductor; and μ_0 is the permeability of the free space. This equation is an approximation that can be used in a high-frequency range where the skin depth is very small. If the frequency is low, the DC resistance must be considered together and the following equivalent resistor equation can be used:

$$R = \sqrt{R_{DC}^2 + R_{AC}^2} \tag{5}$$

The modeling frequency is determined based on the relative sizes of R_{DC} and R_{AC}, which are related to the cross-sectional area and the conductivity of the wire or the ball.

The self-partial inductance of a wire with the radius r_w and the length l is calculated as follows [26]:

$$L_p = 2\times10^{-7} l\left[ln\left[\left(\frac{l}{r_w}\right)+\sqrt{\left(\frac{l}{r_w}\right)^2+1}\right] - \sqrt{1+\left(\frac{r_w}{l}\right)^2}+\frac{r_w}{l}\right] \tag{6}$$

The self-inductance of the wire structure has frequency dependence because of the decrease in the internal inductance. However, when the radius of the wire is very small in comparison with the length, and the dielectric constant of the wire is also small, the changes in the self-inductance due to the frequency can almost be neglected.

The capacitance (C) was calculated using the following equation [27]:

$$C = \frac{2\pi\epsilon l}{\operatorname{arcosh}\left(\frac{d}{a}\right)}, \tag{7}$$

where a is the wire radius; d is the distance; l is the wire length; and ϵ is the permittivity. This capacitance equation is established between a conductor with a circular cross-sectional area and the ideal ground. It cannot be generally applied when another conductor exists nearby, but it can be used approximately when the ground capacitance is dominant. If the dielectric constant is preserved according to the frequency, the capacitance equation is independent of the frequency. In addition, if the loss factor is considered in the permittivity of the PCB or the packaging medium, the conductance term also needs to be considered.

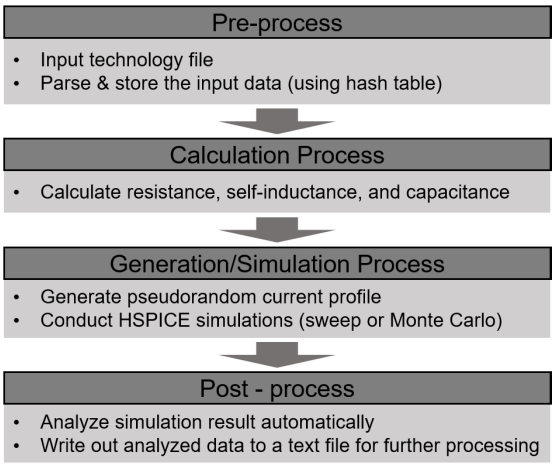

FIGURE 7. Procedure of our proposed fast analysis methodology for PI.

III. PROCEDURE OF PROPOSED METHODOLOGY

This section describes in detail the PI coanalysis methodology. As shown in Figure 7, we first read the PDN and simulation parameters and internally computes the RLC values in pre-calculations process. The PDN model is simulated using the S-parameter. If we directly input the lumped RLC value

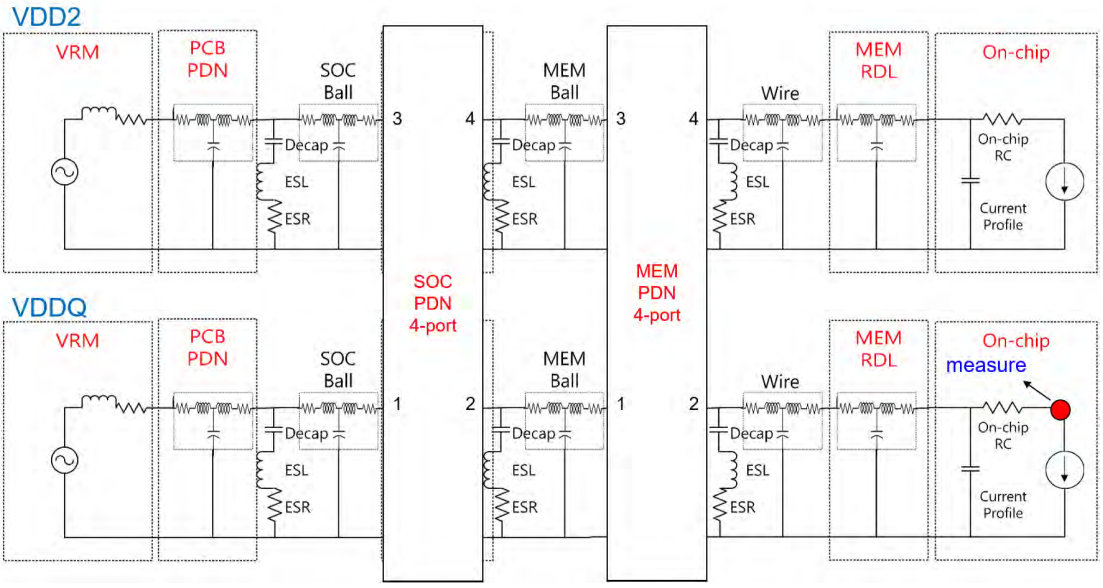

FIGURE 8. Schematic of PoP PDS model and measurement point for on-chip PI analysis.

of the PDN, the generated lumped RLC PDN model and the remaining parameters are parsed. In addition, an on-chip current profile is generated based on the input parameters. All the simulation results are automatically summarized in the output file.

In our PDS model, PI can be analyzed using two methods that change the design and process parameters: sweep simulation and Monte Carlo simulation. In sweep simulation, we observe how each parameter affects the PI characteristics. The variation in the IR drop of the on-chip can be observed by sweeping one parameter. This allows us to analyze the relative impact of the different parameters and the trends of the linear and nonlinear effects. Monte Carlo simulation is mainly performed to investigate how the errors in the process affect the entire PDS. For example, when the geometric dimension of the memory package PDN varies, Monte Carlo simulation can be used for PI analysis. In addition, our proposed methodology enables fast statistical analysis of simultaneous process/voltage/temperature changes through massive Monte Carlo simulations. Both the sweep and Monte Carlo methods are applicable for transient and AC simulations.

IV. SIMULATION AND ANALYSIS

Our proposed methodology is written in *Perl* and *Synopsys HSPICE* [28], and the PDN model is extracted from the *HFSS* tool [29]. We validate using a 2.4GHz Intel Xeon E5-2620V3 Linux workstation with a single core for the *SPICE* simulation. We compare our proposed methodology with the full layout SPICE transient simulation, and perform several case-based sweeps and Monte Carlo simulations for PI analysis. Figure 8 shows the simplified schematic of VDDQ and VDD2 of the PoP PDS model. Our multi-domain PDN model is adopted for the SoC and the memory package. We use PDN of the PCB board as the lumped RLC element with actual parameter values. All the simulations are measured at the pad of the on-chip to analyze the power transfer from the VRM to the memory chip (see Figure 8). The nominal value of the important parameters and the VDD (VDDQ/VDD2) noise values are described in Table 3. Other parameters have less effect on the results; therefore, we set the other parameters based on the 800MHz LPDDR4 memory environment.

TABLE 3. Values of the used parameters that significantly affect the simulation results.

Parameter types	Names	Nominal values	Units
General model	On_Chip_R	20	mohm
	On_Chip_C	0.06	nF
Current profile	Time_length	80	ns
	Delay_VDDQ	20	ns
	Interval_VDDQ	0	ps
	Slope_step_ MIN/MAX_VDDQ	50/60	ps
	I_MIN/MAX_VDDQ	6/18	mA
	Delay_VDD2	20	ns
	Interval_VDD2	0	ps
	Slope_step_ MIN/MAX_VDD2	50/100	ps
	I_MIN/MAX_VDD2	9/50	mA
VRM	VDDQ_nom	1.1	V
	VDDQ_noise	0	V
	VDDQ_freq	500	MHz
	VDD2_nom	1.1	V
	VDD2_noise	0.011	V
	VDD2_freq	500	MHz

A. MODEL VERIFICATION

We verify our proposed methodology using the PoP PDS model with the SPICE simulation results of the full industrial layout.[3] under the JEDEC LPDDR4 environment. The main

[3]The full layout design is not made public for security reasons; therefore, we received comparison simulation results as the peak-to-peak ripple voltage values for industrial design.

TABLE 4. Comparison of peak-to-peak ripple voltage results obtained by full layout SPICE simulation and proposed methodology.

Peak-to-peak ripple voltage		
	Full layout SPICE (mV)	Proposed (mV)
Core	15.41	17.72
I/O	9.0	8.0
	Full layout SPICE	Proposed
Average Runtime	7200s	7.0s

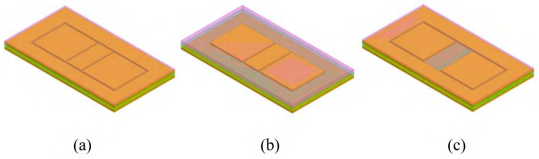

FIGURE 9. Slant view of the structure of the multi-domain PDN according to existence of the ring and central ground planes. (a) PDN structure with both the ring and central ground planes (RGND = 1 and CGND = 1) (b) PDN structure with the central ground only (RGND = 0 and CGND = 1) (c) PDN structure with the ring ground only (RGND = 1 and CGND = 0).

parameters used in the experiment are shown in Table 3, and the core (VDDQ) and I/O (VDD2) peak-to-peak ripple voltage are compared in the 800MHz IC switching-frequency environment. In this experiment, we extract the lumped RLC values of PCB and RDL. In addition, we extract the four-port S-parameters of SoC and memory PDN. The lumped RLC values of the ball and wire are calculated based on the real structure, and the same current profile is used for comparison. Table 4 shows that the core and I/O peak-to-peak ripple voltages are 1.40% and 0.82%, respectively, for the full layout SPICE simulation, 1.61% and 0.73%, respectively for our model with respect to the reference voltage (1.1V). The main cause of the error is the difference in considering the parasitic RLC in the model. However, the acceptable error range with the consideration of the reference VDD is 1.1V, and the generally permissible peak-to-peak ripple voltage is 4-10%. Thus, using our proposed methodology, it is possible to analyze the PI using parametric link simulations with a runtime that is 1,000 times faster.

B. DOMAIN COUPLING

To investigate the domain coupling effect of the ring and the central ground plane, we simulate two methods. First, we analyze the effect of the existence of the central and ring grounds. Figure 9 shows our three cases of the PDN structures in SoC and memory package: RGND = 1 and CGND = 1, RGND = 1 and CGND = 0, and RGND = 0 and CGND = 1. Figure 10(a) is the generated current profile. As shown in Figure 10(b), both the central and ring grounds can reduce the domain-coupling effect by reducing the mutual capacitance between the two domains. In this case, the central ground plane improves PI more effectively than the ring ground plane. Second, we vary the width of the ground plane margin from $0\mu m$ to $3{,}000\mu m$ with the other parameters remaining fixed: CGND = 1, RGND = 0.

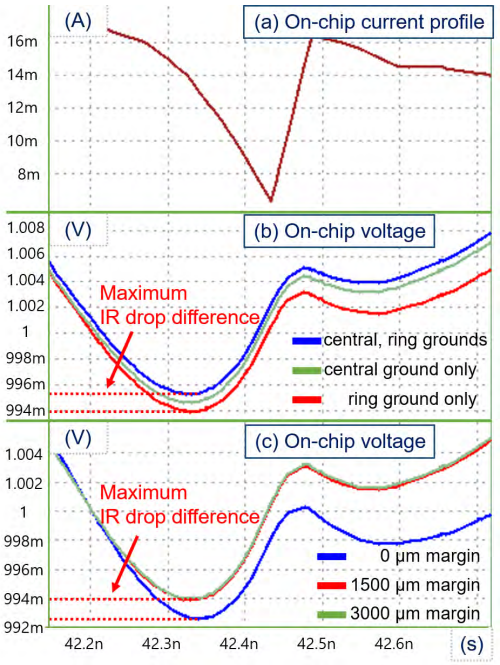

FIGURE 10. Transient result of (a) generated current profile and corresponding voltage fluctuations in two methods (b) voltage with three PDN structures (with both center/ring, without ring, without the central ground) and (c) three ground margins ($0\mu m$, $1500\mu m$, $3000\mu m$) of the package PDN on the pad of the on-chip VDDQ.

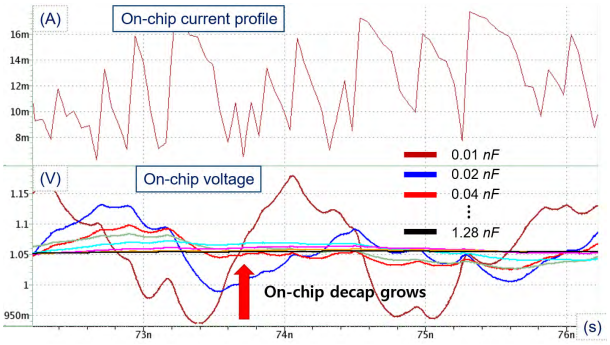

FIGURE 11. Current profile (above) and voltage graph (below) on the pad of the on-chip VDDQ. IR drop on the on-chip pad decreases as the on-chip decap increases.

As shown in Figure 10(c), we observe that the large margin width can reduce the IR drop. Note that our multi-domain PDN model is relatively smaller than the real-package PDN structure. Therefore, the effect of the domain coupling is also less than the realistic environment.

C. ON-CHIP DECAP EFFECT

In general, decap is used to improve PI in various PDS. However, a large decap is expensive and changes the resonance frequency of the system. Therefore, we perform sweep simulation by varying the on-chip decap to determine the proper decap ranging from $0.01nF$ to $1.28nF$. As shown in Figure 11, the large decap effectively reduces the high-frequency VDD ripple of the on-chip pad. Moreover, we investigate the proper size of the decap from the sweep simulation (see Figure 12),

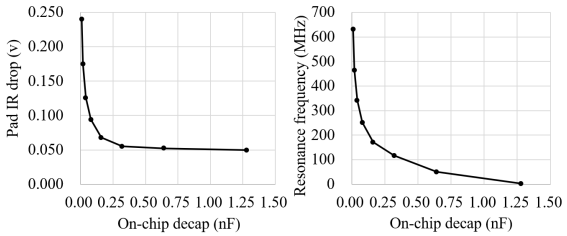

FIGURE 12. IR drop (left) and resonance frequency (right) on the pad of on-chip with various values of the on-chip decap.

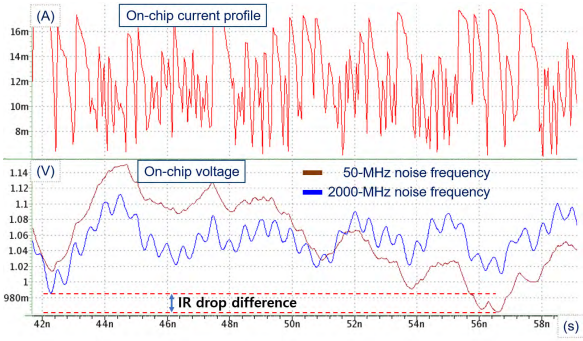

FIGURE 13. Transient result of the voltage (above) and the current profile (below) on the pad of the on-chip VDDQ.

which considers the resonance frequency of the PDS with the AC simulation. The 0.06*n*F on-chip decap used as an industrial reference is a reasonable value because 0.06*n*F of the decap effectively reduces the IR drop and produces approximately 250MHz of resonance frequency for the PDS. The resonance frequency of 250MHz is small as compared with the IC switching frequency of the experimental environment. However, PI may be worse if other frequency noises overlap the PDS resonance frequency. Therefore, it is necessary to analyze the input VRM noise of various frequencies to investigate the effect of the resonance frequency.

D. INPUT NOISE EFFECT

To analyze the effect of the input VDD noise frequency, we use a simulation with our proposed methodology. Although the magnitude of the input noise is the same, the PI depends on the frequency.[4] As shown in Figure 13, the effect of the input noise is based on the frequency of the VDDQ of the on-chip pad. In addition, we can analyze the trend of the relationship between the IR drop and the input VDDQ noise frequency, as shown in Figure 14(a). Moreover, we analyze how the critical noise frequency range (see the red circle in Figure 14(a)) affects the PI. We perform 1,000 Monte Carlo simulations with 10% 1-sigma variation, as shown in Figure 14. The total simulation runtime

[4]Generally, low/middle-range frequency noise is effectively controlled by on-chip decaps of PCB and packages. However, in this experiment, the decaps are ignored to observe the clear difference of the on-chip VDD fluctuation. In this experiment, we sweep the input noise frequency of VDDQ with the same VDD offset.

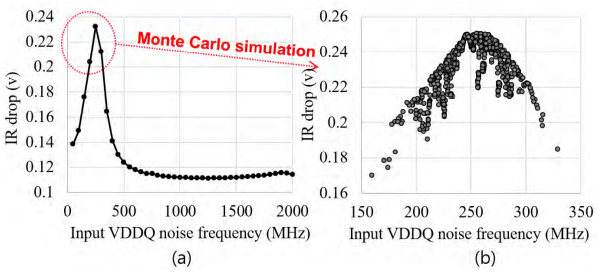

FIGURE 14. IR drop on the on-chip pad with various input noise frequencies; (a) sweep simulations with 100MHz step, (b) Monte Carlo simulations.

is approximately 120 min, which is significantly faster than the traditional full-layout simulations. As stated in Subsection IV-C, the PDS has a resonance frequency of 250MHz, and the on-chip IR-drop is the worst when the input noise frequency is equal to the resonance frequency (see Figure 14). Therefore, the proposed methodology can be a design guideline for a specific input noise, such as determining the appropriate on-chip decap size based on the VRM input noise or changing the RDL structure based on the results of the on-chip simulations.

V. CONCLUSION

In this study, we propose a fast PI coanalysis methodology for a multi-domain high-speed memory system. Our methodology has several advantages over the conventional full-layout SPICE-based analysis and the case-specific design model-based analysis. First, our methodology improves the simulation flexibility and the runtime with a pseudo-randomized current profile generation that characterizes the realistic switching current. Second, our PI analysis is fast and has massive parametric link simulations. Third, we consider the structural changes of PDN using multiple power domains to analyze the domain coupling effect. We compare our PDS model and our proposed methodology with the results of the industrial full-layout SPICE simulation. Our experimental studies confirm the PI improvement by the structural changes of the ground plane in a multiple power domain PDN. Moreover, we determine an proper on-chip decap value based on the resonance frequency under the LPDDR4 800MHz environment by using fast Monte Carlo analysis. Thus, our proposed PI coanalysis methodology can be used by high-speed memory package designers as a design guideline to predict PI.

ACKNOWLEDGMENT

This paper was presented at the 2018 Design, Automation & Test in Europe Conference & Exhibition (DATE) [1].

REFERENCES

[1] S. Kim, K. J. Han, Y. Kim, and S. Kang, "Fast chip-package-PCB coanalysis methodology for power integrity of multi-domain high-speed memory: A case study," in *Proc. DATE*, 2018, pp. 885–888.
[2] S. Lee, H. Cho, Y. H. Son, Y. Ro, N. S. Kim, and J. H. Ahn, "Leveraging power-performance relationship of energy-efficient modern DRAM devices," *IEEE ACCESS*, vol. 6, pp. 31387–31398, 2018.

[3] M. Swaminathan and E. engin, *Power Integrity Modeling and Design for Semiconductors and Systems*. Upper Saddle River, NJ, USA: Prentice-Hall, 2007, pp. 24–45.
[4] S. L. Huh and H. Shi, "Detection of noise coupling between power domains on package," in *Proc. ECTC*, 2016, pp. 2028–2033.
[5] *JEDEC LPDDR4 Standard*. Accessed: Apr. 7, 2017. [Online]. Available: https://www.jedec.org/sites/default/files/docs/JESD209-4.pdf
[6] Z. Zeng, X. Ye, Z. Feng, and P. Li, "Tradeoff analysis and optimization of power delivery networks with on-chip voltage regulation," in *Proc. DAC*, 2010, pp. 831–836.
[7] D.-H. Lee, Y.-S. Shin, C.-G. Kim, J.-H. Song, J.-K. Wee, J.-M. Lee, and J.-S. Seol, "Design of multiple power domains based on ground separation technique for low-noise and small-size module," in *Proc. APEMC*, 2012, pp. 805–808.
[8] M. E. Kowalski and P. Codd, "Co-simulation of IC, package and PCB power delivery networks in ultra-low voltage power rail designs," in *Proc. ECTC*, 2007, pp. 798–803.
[9] Y.-M. Lee and C. C. P. Chen, "The power grid transient simulation in linear time based on 3-D alternating-direction-implicit method," *IEEE Trans. Comput.-Aided Design Integr.*, vol. 22, no. 11, pp. 1545–1550, Nov. 2003.
[10] M.-C. Hsieh, "Advanced flip chip package on package technology for mobile applications," in *Proc. ICEPT*, 2016, pp. 486–491.
[11] D. M. Mathew, M. Schultheis, C. C. Rheinländer, C. Sudarshan, C. Weis, N. Wehn, and M. Jung, "An analysis on retention error behavior and power consumption of recent DDR4 DRAMs," in *Proc. DATE*, 2018, pp. 293–296.
[12] J. Kim, W. Lee, Y. Shim, J. Shim, K. Kim, J. S. Pak, and J. Kim, "Chip-package hierarchical power distribution network modeling and analysis based on a segmentation method," *IEEE Trans. Adv. Packag.*, vol. 33, no. 3, pp. 647–659, Aug. 2010.
[13] J. Feng, B. Dhavale, J. Chandrasekhar, Y. Tretiakov, and D. Oh, "System level signal and power integrity analysis for 3200 Mbps DDR4 interface," in *Proc. ECTC*, 2013, pp. 1081–1086.
[14] K. Jeong, A. B. Kahng, S. Kang, T. S. Rosing, and R. Strong, "MAPG: Memory access power gating," in *Proc. DATE*, 2012, pp. 1054–1059.
[15] H.-H. Chuang, W.-D. Guo, Y.-H. Lin, H.-S. Chen, Y.-C. Lu, Y.-S. Cheng, M.-Z. Hong, C.-H. Yu, W.-C. Cheng, Y.-P. Chou, C.-J. Chang, J. Ku, T.-L. Wu, and R.-B. Wu, "Signal/power integrity modeling of high-speed memory modules using chip-package-board coanalysis," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 381–391, May 2010.
[16] B. Bae, S. Kim, Y. Kim, S. Kang, I. J. Kim, K. Kim, S. Kang, and K. J. Han, "A preliminary analysis of domain coupling in package power distribution network," in *Proc. RFIT*, 2017, pp. 19–21.
[17] Y. Panov and M. M. Jovanovic, "Design considerations for 12-V/1.5-V, 50-A voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 16, no. 6, pp. 776–783, Nov. 2001.
[18] E. H.-K. Hsiung, Y.-L. Li, R.-B. Wu, T. Su, Y. S. Cheng, and K. B. Wu, "A linear 4-element model of VRM—Characteristics, practical uses and limitations," in *Proc. EDAPS*, 2012, pp. 13–16.
[19] K. L. Kaiser, *Electromagn. Compat. Handbook*, CRC press, 2004, chapter 8.
[20] ANSYS. *CPM*. Accessed: Nov. 14, 2016. [Online]. Available: http://www.ansys.com
[21] B. Ross, "IBIS models for signal integrity applications," *EE Times*, vol. 18, no. 9, pp. 38–43, 1996.
[22] R. Stilkol, "Chip-package-system (CPS) co-design verification," in *Proc. ChipEx*. Oakland, CA, USA: ASG, 2011.
[23] J. Kim, S. Wu, H. Wang, Y. Takita, H. Takeuchi, K. Araki, G. Feng, and J. Fan, "Improved target impedance and IC transient current measurement for power distribution network design," in *Proc. EMC*, 2010, pp. 445–450.
[24] Y.-E. Chen, T.-H. Tsai, S.-H. Chen, and H.-M. Chen, "Cost-effective decap selection for beyond die power integrity," in *Proc. DATE*, 2014, pp. 1–4.
[25] W. Hayt and J. Buck, *Engineering Electromagnetics*. New York, NY, USA: McGraw-Hill, 1981, ch. 13.
[26] R. C. Paul, "What is 'partial inductance'?" in *Proc. EMC*, 2008, pp. 1–23.
[27] J. D. Jackson, *Classical Electrodynamics*. Hoboken, NJ, USA: Wiley, 1975, p. 80.
[28] Synopsys. (2013). *HSPICE, Version K-2015.06-2*. [Online]. Available: http://www.synopsys.com
[29] ANSYS. (2013). *HFSS, Version 16.2*. [Online]. Available: http://www.ansys.com

SEUNGWON KIM (S'15) received the B.S. degree in electrical engineering from the Ulsan National University of Science and Technology (UNIST), Ulsan, South Korea, in 2014, where he is currently pursuing the Ph.D. degree in electrical engineering. His current research interests include power delivery network optimization and low power physical design optimization.

KI JIN HAN (S'06–M'10–SM'16) received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1998 and 2000, respectively, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2009.

He was with the System Research and Development Laboratory, LG Precision Company, Ltd., Yongin, South Korea, from 2000 to 2005. From 2009 to 2011, he was with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA, as a Postdoctoral Researcher. He is currently an Associate Professor with the Division of Electronics and Electrical Engineering, Dongguk University, Seoul. His current research interests include computational electromagnetics, electromagnetic compatibility and reliability for power electronics, signal/power integrity for high-speed digital design, antennas, and electrical modeling of electronic packaging and interconnections.

Dr. Han was a recipient of the Samsung Scholarship for graduate study, in 2005 and the 2015 IEEE TCPMT Best Paper Award, in 2016. He served as the Guest Editor of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY (TCPMT), in 2018, and the Technical Program Committee Chair of the 2015 IEEE Electrical Design of Advanced Packaging and Systems Symposium.

YOUNGMIN KIM (M'02) received the B.S. degree in electrical engineering from Yonsei University, Seoul, Korea, in 1999, and the M.S. and Ph.D. degrees in electrical engineering from the university of Michigan, Ann Arbor, in 2003 and 2007, respectively.

He has held a senior engineer position at Qualcomm, San Diego, CA. He is currently an Associate Professor with Hongik University, Seoul. Prior to joining Hongik University, he was with Kwangwoon University, Seoul, and with the School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology (UNIST), Ulsan, South Korea. His research interests include embedded-systems, variability-aware design methodologies, design for manufacturability, design and technology co-optimization methodologies, and low-power and 3D IC designs.

SEOKHYEONG KANG (S'11–M'13) received the B.S. and M.S. degrees in electrical engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 1999 and 2001, respectively, and the Ph.D. degree from the VLSI CAD Laboratory, University of California at San Diego, La Jolla, USA, in 2013.

He was with the System-on-Chip (SoC) Development Team, Samsung Electronics, Suwon, South Korea, from 2001 to 2008, where he was involved in development and commercialization of optical disk drive SoC. He was a Professor with the Department of Electrical Engineering, Ulsan National Institute of Science and Technology, Ulsan, South Korea, from 2014 to 2018. He has been a Professor with the Department of Electrical Engineering, Pohang University of Science and Technology, since 2018. His current research interests include low power design optimization and cost-driven methodology for chip implementation.