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Variability study of Si nanowire FETs with different junction gradients

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Random dopant fluctuation effects of gate-all-around Si nanowire field-effect transistors (FETs) are investigated in terms of different diameters and junction gradients. The nanowire FETs with smaller diameters or shorter junction gradients increase relative variations of the drain currents and the mismatch of the drain currents between source-drain and drain-source bias change in the saturation regime. Smaller diameters decreased current drivability critically compared to standard deviations of the drain currents, thus inducing greater relative variations of the drain currents. Shorter junction gradients form high potential barriers in the source-side lightly-doped extension regions at on-state, which determines the magnitude of the drain currents and fluctuates the drain currents greatly under thermionic-emission mechanism. On the other hand, longer junction gradients affect lateral field to fluctuate the drain currents greatly. These physical phenomena coincide with correlations of the variations between drain currents and electrical parameters such as threshold voltages and parasitic resistances. The nanowire FETs with relatively-larger diameters and longer junction gradients without degrading short channel characteristics are suggested to minimize the relative variations and the mismatch of the drain currents. © *2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).*
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Random dopant fluctuation (RDF) is one of the significant variability problems in the nanoscale field-effect transistors (FETs).[1–3] Even non-planar MOSFETs such as FinFETs and gate-all-around (GAA) Si nanowire FETs suffer from the fluctuations of short channel characteristics and on/off-state currents as discrete dopants implanted at highly-doped source/drain (S/D) regions penetrate into the S/D extension and the channel regions.[4–6]

Recently, the nanoscale FETs adapting steep junction gradients (L_j) and lightly-doped underlap structure are suggested to minimize gate-induced drain leakage and short channel degradation, and to improve AC performance by reducing parasitic capacitances.[7,8] Especially, GAA Si nanowire FETs have great potential to enable short channel immunity and DC/AC performance enhancement by encircling all around the channel under 7-nm regime.[9] Therefore, the analysis for RDF effects to GAA Si nanowire FETs with different L_j values is significant to provide the device design guideline to optimize both DC/AC performance and variability concerns.

In this work, the RDF effects induced by highly-doped S/D regions of Si nanowire FETs with different diameters (D_{NW}) and L_j values were investigated in terms of the drain currents (I_{ds}) in both linear and saturation regimes. Variability origins of the I_{ds} were analyzed by comparing correlations of the I_{ds} with threshold voltages (V_{th}) and S/D parasitic resistances (R_{sd}). We also investigated the mismatch of the I_{ds} between source-drain and drain-source bias change to consider the interchangeability between source and drain terminals.

GAA Si nanowire FETs were simulated using Sentaurus TCAD[10] by solving drift-diffusion (DD) equations coupled to Poisson and carrier continuity equations self-consistently. Density-gradient model was also adapted to consider quantum confinement effects inside the nanowire channels due

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to its shorter computation time compared to Schrodinger equations for variability study. Impurity scattering, velocity saturation, and surface roughness scattering were also considered using three basic mobility models: Philips unified mobility model, Canali model, and Lombardi model, respectively, which were equivalent to the previous RDF study.[6] All the n-type nanowire FETs had the same arsenic doping concentrations of 10^{20} cm^{-3} at the S/D regions with the fixed length (L_{sd}) of 5 nm. Nanowire channels were lightly-doped with boron of 10^{16} cm^{-3} to concentrate on the impact of arsenic discrete dopants on the RDF effects.[11] All the nanowire FETs had the same physical gate length (L_{gate}) of 20 nm, SiO_2 thickness (t_{ox}) of 1 nm, and S/D extension lengths (L_{EXT}) of 6 nm. RDF effects were analyzed using the nanowire FETs with different D_{NW} values of 5 and 9 nm, and different L_j values of 0.5, 1.5, and 2.0 nm/dec which were possible to be formed at single-crystal Si material[12] or at multi-gate structure.[13] Device structure and doping profiles of the simulated nanowire FETs were specified in Fig. 1.

RDF effects were investigated using Sano model, adapting long-range and short-range Coulomb potentials separately to consider DD transport and Coulomb scattering, respectively.[14] Screening factor is defined as $2\times N^{1/3}$, where N is arsenic doping concentration. Because all the nanowire channels were lightly-doped with boron, only the arsenic dopants were randomized. The number of samples for RDF study was 250 for each D_{NW} and L_j. Gate voltage (V_{gs}) was applied from 0 to 1 V, whereas drain voltage (V_{ds}) was applied at 0.05 and 0.7 V in the linear and saturation regimes, respectively. Source and drain terminals were interchanged and indicated as forward-bias (source-referenced) and reverse-bias (drain-referenced) conditions. Linear on-currents ($I_{ds,lin}$) were measured at V_{ds} of 0.05 V, and saturation on-currents ($I_{ds,sat}$) were measured at V_{ds} of 0.7 V. V_{th} values were extracted using the constant current method at $I_{th} = W_{eff}/L_{gate}\times 10^{-8}$, where W_{eff} is the perimeter of nanowire channel ($W_{eff} = D_{NW}\times\pi$). R_{sd} values were extracted using Y-function technique,[15] applicable to the nanowire FETs with D_{NW} smaller than 10 nm due to volume inversion effects neglecting surface roughness scattering within the channel regions in the inversion regimes.[16] One example for transfer characteristics and Y-function curves of the nanowire FETs with the D_{NW} of 5 nm and the L_j of 0.5 nm/dec in the forward-bias condition was shown in Fig. 2. Y-functions satisfied the linearity conditions in the strong inversion regime, which were valid to extract R_{sd} of the nanowire FETs effectively.

Figure 3 showed the average values of V_{th} for the nanowire FETs with different D_{NW} and L_j at V_{ds} of 0.05 and 0.7 V. As L_j increased, the number of S/D dopants penetrating into the channel regions increased, thus decreasing V_{th} values. V_{th} changes for different L_j was smaller for the D_{NW} of 5 nm than for the D_{NW} of 9 nm because the nanowire FETs with smaller D_{NW} had greater gate-to-channel controllability. Although V_{th} variation increased as D_{NW} or L_j increased, the maximum standard deviation of V_{th} was negligibly small as 2.5 mV.

Figure 4 showed the relative variations of $I_{ds,lin}$ and $I_{ds,sat}$ of the nanowire FETs with D_{NW} of 5 and 9 nm. Relative variations were calculated as the standard deviations divided by the averages. Standard deviations of the I_{ds} increased as D_{NW} or L_j increased, similar to the RDF study for the

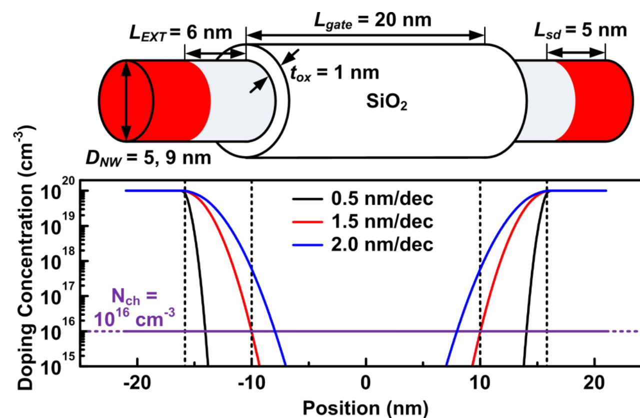

FIG. 1. Device structure and doping profiles of the nanowire FETs with different diameters (D_{NW}) of 5 and 9 nm and junction gradients (L_j) of 0.5, 1.5, and 2.0 nm/dec.

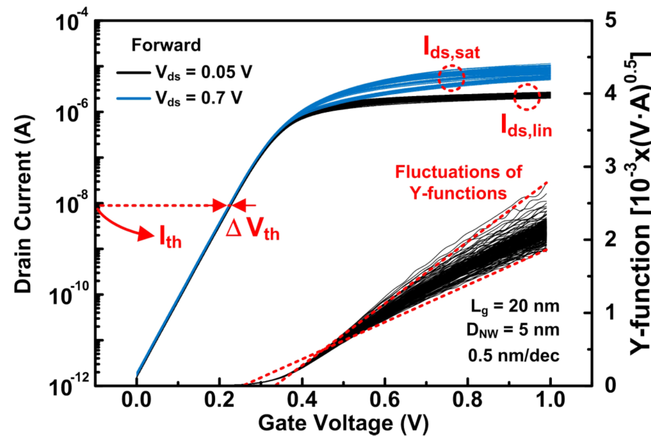

FIG. 2. One example for transfer characteristics at drain voltages of 0.05 and 0.7 V and Y-function curves of the nanowire FETs with D_{NW} of 5 nm and L_j of 0.5 nm/dec.

D_{NW} and L_{EXT} splits.[6] The nanowire FETs with the D_{NW} of 5 nm showed greater relative variations of $I_{ds,sat}$ than did those with the D_{NW} of 9 nm, following Pelgrom's law; greater relative variations of DC performance as the gate lengths or widths of planar MOSFETs decreased.[17] The relative variations of $I_{ds,lin}$ were within the range below 9 % for all V_{gs} values, significantly smaller than the relative variations of $I_{ds,sat}$. Slightly-increased relative variations of I_{ds} at off-state for larger D_{NW} or greater L_j were due to less gate-to-channel controllability and more number of arsenic dopants permeating into the channel regions, respectively. Increased mismatch of the $I_{ds,lin}$ at off-state for the D_{NW} of 5 nm and the L_j of 2.0 nm/dec was because some nanowire FETs had extremely-short undoped channel regions at the edge of source or drain terminals, thus even the V_{ds} of 0.05 V under high gate-to-channel controllability affected $I_{ds,lin}$ at off-state differently between forward- and reverse-bias conditions. But the significant viewpoint was that shorter L_j of the nanowire FETs induced greater relative variations of $I_{ds,sat}$, indicated as the shaded regions in Fig. 3(b).

The nanowire FETs with the L_j of 0.5 nm/dec had high potential barriers (Φ_B) in the source-side extension regions even at on-state, obeying thermionic-emission (TE) mechanism as shown in Fig. 5. TE currents are exponentially proportional to the Φ_B.[18] The Φ_B values of the nanowire FETs with the L_j of 0.5 nm/dec having the smallest and greatest $I_{ds,sat}$ were 55 and 16 meV, respectively, whereas the maximum Φ_B value of the nanowire FETs with the L_j of 2.0 nm/dec was 19 meV, which was smaller than the thermal energy (25 meV) at room temperature (300 K). Thus, electrons

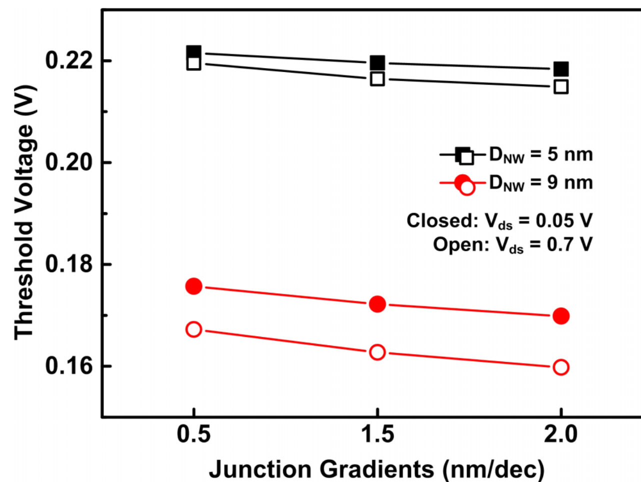

FIG. 3. Average values of V_{th} for the Si nanowire FETs with different D_{NW} and L_j in both linear and saturation regimes.

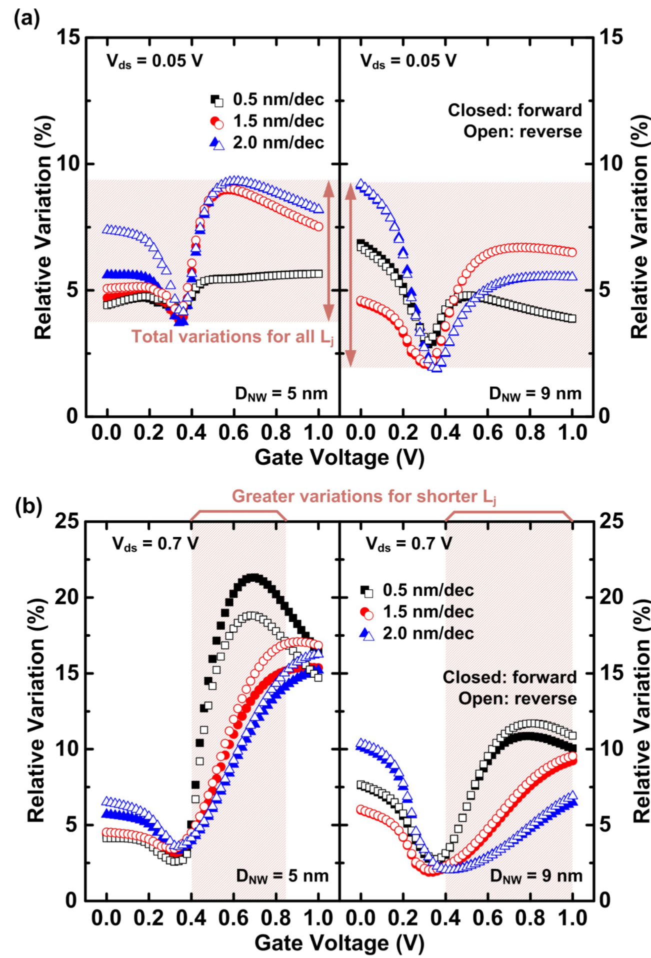

FIG. 4. Relative variations of the drain currents ($I_{ds,lin}$, $I_{ds,sat}$) for the nanowire FETs with all different D_{NW} and L_j in (a) linear and (b) saturation regimes. Forward- and reverse-bias conditions were specified as the closed and open symbols, respectively. Shaded regions in (a) indicated the total relative variations of $I_{ds,lin}$, whereas those in (b) indicated that shorter L_j induced greater relative variations of $I_{ds,sat}$.

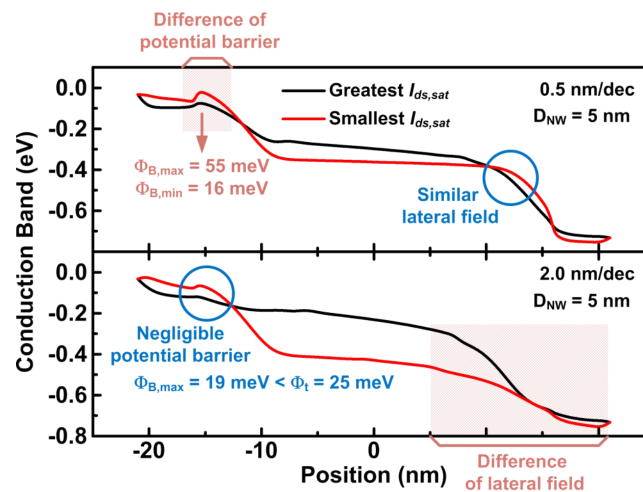

FIG. 5. Conduction energy band diagrams at the center of nanowire FETs with the D_{NW} of 5 nm and the L_j of 0.5 and 2.0 nm/dec at on-state condition as the nanowire FETs had the greatest (black) and smallest (red) $I_{ds,sat}$ in the reverse-bias condition.

in the nanowire FETs with the L_j of 2.0 nm/dec move from source to drain regions freely without being impeded by the Φ_B at on-state. The relative variations of $I_{ds,sat}$ for the L_j of 2.0 nm/dec were determined by the lateral field near the drain regions, indicated as the shaded regions in the bottom of Fig. 5. The nanowire FET with the L_j of 2.0 nm/dec having the greatest $I_{ds,sat}$ had higher later field than that having the smallest $I_{ds,sat}$. But the relative variations of $I_{ds,sat}$ for the L_j of 0.5 nm/dec showed similar lateral fields near the drain regions between the greatest and the smallest $I_{ds,sat}$.

These explanations were verified by investigating the variability origins of $I_{ds,sat}$ in the inversion regimes, as shown in Fig. 6. Correlation coefficients (ρ) were calculated using Spearman's correlations.[5] As the L_j increased from 0.5 to 2.0 nm/dec, the variations of $I_{ds,sat}$ were much correlated with the variations of R_{sd} but less correlated with the variations of V_{th}. For the L_j of 0.5 nm/dec, both $I_{ds,sat}$ as well as $V_{th,sat}$ were determined by the Φ_B in the source-side extension regions. For the L_j of 2.0 nm/dec, on the other hand, highly-doped S/D extension regions reduced the Φ_B and instead affected the lateral field near the drain regions as shown in Fig. 4. Because the lateral field was reduced by R_{sd}, the variations of R_{sd} induced the variations of $I_{ds,sat}$ for the L_j of 2.0 nm/dec greatly. The nanowire FETs with the D_{NW} of 9 nm and L_j of 1.5 and 2.0 nm showed similar correlations of $I_{ds,sat}$ with $V_{th,sat}$ and R_{sd}, different from those with the D_{NW} of 5 nm. As the D_{NW} increased from 5 to 9 nm, smaller gate-to-channel controllability induced much drain-induced barrier lowering (DIBL) effects, reducing Φ_B and correlations of $I_{ds,sat}$ with $V_{th,sat}$ for L_j of both 1.5 and 2.0 nm/dec.

Figure 7 showed the $I_{ds,sat}$ mismatch of the nanowire FETs with D_{NW} of 5 and 9 nm. The mismatch was calculated as difference of the $I_{ds,sat}$ between forward- and reverse-bias conditions divided by the $I_{ds,sat}$ in the forward-bias condition. The mismatch values were greater for smaller

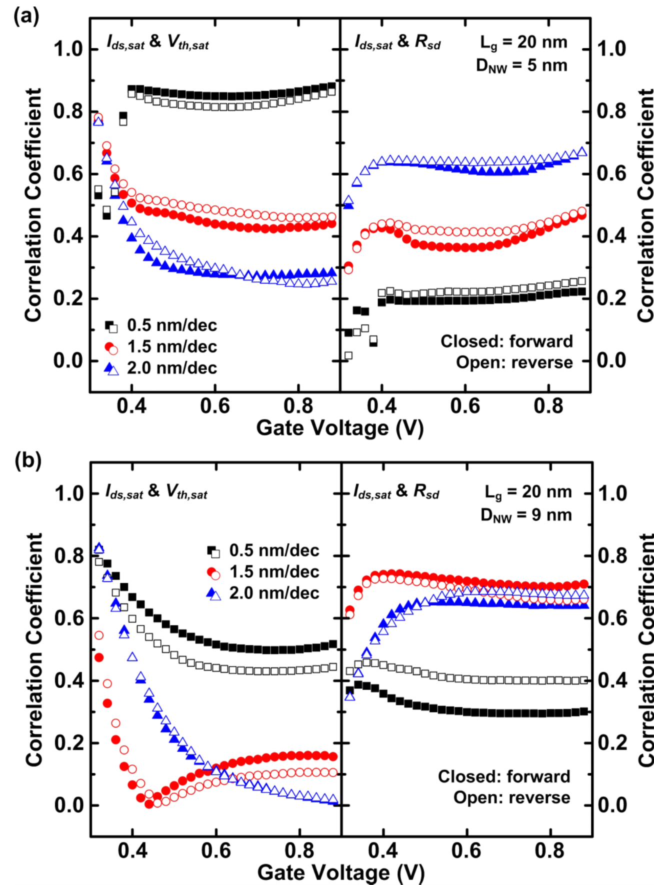

FIG. 6. Spearman correlation coefficients of $I_{ds,sat}$ with $V_{th,sat}$ and R_{sd} for the nanowire FETs with D_{NW} of (a) 5 nm and (b) 9 nm.

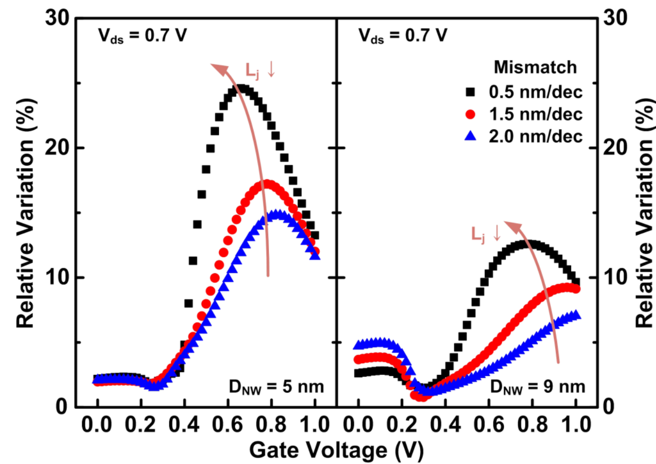

FIG. 7. Mismatch of the $I_{ds,sat}$ between forward- and reverse-bias conditions for the nanowire FETs with D_{NW} of 5 and 9 nm.

D_{NW} or shorter L_j, especially in the inversion regimes. The $I_{ds,sat}$ mismatch was induced by difference of the arsenic doping concentrations between source- and drain-side extension regions. Φ_B was affected by the doping concentrations at the source-side extension regions only, whereas R_{sd} was affected by the doping concentrations at any side of the extension regions. For the D_{NW} of 9 nm, DIBL effects lowered the Φ_B at on-state, thus the Φ_B values between source- and drain-side extension regions were not much different compared to those for the D_{NW} of 5 nm. For the longer L_j, because the $I_{ds,sat}$ were affected by R_{sd} rather than Φ_B, the $I_{ds,sat}$ mismatch of the nanowire FETs decreased. Thus, in terms of the relative variations and the $I_{ds,sat}$ mismatch, the nanowire FETs with relatively-larger D_{NW} and longer L_j were promising to minimize the variability problems.

RDF effects of the GAA Si nanowire FETs were investigated in terms of different D_{NW} and L_j splits. Relative variations of $I_{ds,sat}$ at on-state increased with decreasing the D_{NW} or the L_j due to Pelgrom's law and TE mechanism, exponentially-proportional to the Φ_B, respectively. Because of this physical phenomena, the variations of $I_{ds,sat}$ were more correlated with the variations of $V_{th,sat}$ but less correlated with the variations of R_{sd} as the L_j decreased. The $I_{ds,sat}$ mismatch between forward- and reverse-bias conditions increased as the D_{NW} or the L_j decreased because the Φ_B depended greatly on the doping concentrations at the source-side extension regions only. Therefore, the nanowire FETs with larger D_{NW} and longer L_j enough to maintain short channel immunity were promising to minimize the variability and mismatch problems.

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[1] M. F. Bukhori, S. Roy, and A. Asenov, IEEE Trans. Electron Devices **57**, 795 (2010).
[2] G. Leung and C. O. Chui, IEEE Electron Device Lett. **33**, 767 (2012).
[3] S. Markov, B. Cheng, and A. Asenov, IEEE Electron Device Lett. **33**, 315 (2012).
[4] M. Uematsu, K. M. Itoh, G. Mil'nikov, H. Minari, and N. Mori, Tech. Dig. Int. Electron Devices Meet. (2012) pp. 709–712.
[5] K. Nayak, S. Agarwal, M. Bajaj, K. V. R. M. Murali, and V. R. Rao, IEEE Trans. Electron Devices **62**, 685 (2015).
[6] J.-S. Yoon, T. Rim, J. Kim, K. Kim, C.-K. Baek, and Y.-H. Jeong, Appl. Phys. Lett. **106**, 103507 (2015).
[7] P. Kerber, Q. Zhang, S. Koswatta, and A. Bryany, IEEE Electron Device Lett. **34**, 6 (2013).
[8] J.-S. Yoon, E.-Y. Jeong, C.-K. Baek, Y.-R. Kim, J.-H. Hong, J.-S. Lee, R.-H. Baek, and Y.-H. Jeong, IEEE Electron Device Lett. **36**, 994 (2015).
[9] D. Yakimets, G. Eneman, P. Schuddinck, T. H. Bao, M. G. Bardon, P. Raghavan, A. Veloso, N. Collaert, A. Mercha, D. Verkest, A. V.-Y. Thean, and K. D. Meyer, IEEE Trans. Electron Devices **62**, 1433 (2015).

[10] Synopsys, *Sentaurus Device User Guide* (Mountain View, CA, 2013).
[11] J.-P. Colinge, *FinFETs and Other Multi-gate Transistors* (Springer-Verlag, New York, NY, USA, 2008).
[12] J. C. Ho, R. Yerushalmi, Z. A. Jacobson, Z. Fan, R. L. Alley, and A. Javey, Nature Mater. **7**, 62 (2008).
[13] K.-W. Ang, J. Barnett, W.-Y. Loh, J. Huang, B.-G. Min, P. Y. Hung, I. Ok, J. H. Yum, G. Bersuker, M. Rodgers, V. Kaushik, S. Gausepohl, C. Hobbs, P. D. Kirsch, and R. Jammy, Tech. Dig. Int. Electron Devices Meet. 837–840 (2011).
[14] N. Sano, K. Matsuzawa, M. Mukai, and N. Nakayama, Microelectron. Reliab. **42**, 189 (2002).
[15] R.-H. Baek, C.-K. Baek, S.-W. Jung, Y. Y. Yeoh, D.-W. Kim, J.-S. Lee, D. M. Kim, and Y.-H. Jeong, IEEE Trans. Nanotechnol. **9**, 212 (2010).
[16] S.-H. Lee, C.-K. Baek, S. Park, D.-W. Kim, D. K. Sohn, J.-S. Lee, D. M. Kim, and Y.-H. Jeong, IEEE Electron Device Lett. **33**, 1348 (2012).
[17] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, IEEE J. Solid-State Circuits **24**, 1433 (1989).
[18] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (John Wiley & Sons, Inc., New Jersey, NJ, USA, 2007).