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Introduction of WO_3 Layer in a Cu-Based Al_2O_3 Conductive Bridge RAM System for Robust Cycling and Large Memory Window

JIYONG WOO^{1,2}, ATTILIO BELMONTE¹, AUGUSTO REDOLFI¹, HYUNSANG HWANG²,
MALGORZATA JURCZAK¹, AND LUDOVIC GOUX¹

¹ IMEC, Leuven 3001, Belgium

² Department of Material Science and Engineering, Pohang University of Science and Technology, Pohang 790-784, Korea (e-mail: jiyongis@postech.ac.kr)

CORRESPONDING AUTHOR: J. WOO (e-mail: jiyongis@postech.ac.kr)

ABSTRACT In this paper, we optimize a $\text{WO}_3\backslash\text{Al}_2\text{O}_3$ bilayer serving as the electrolyte of a conductive bridge RAM device using a Cu-based supply layer. By introducing a WO_3 layer formed by thermal oxidation of a W plug, the hourglass shape of the conductive filament is desirably controlled, enabling excellent switching behavior. We demonstrate a clear improvement of the microstructure and density of the WO_3 layer by increasing the oxidation time and temperature, resulting in a strong increase of the high-resistance-state breakdown voltage. The high quality WO_3 microstructure allows thus the use of a larger reset pulse amplitude resulting both in larger memory window and failure-free write cycling.

INDEX TERMS Conductive-bridge RAM (CBRAM), endurance, low current operation, memory window.

I. INTRODUCTION

Conductive Bridge RAM (CBRAM) has been considered to be a promising candidate to replace NAND FLASH memory because of its high scalability and low power consumption [1]. The resistive switching phenomenon in a CBRAM device is based on electrochemical redox mechanisms between an ionizable metal (Cu and Ag) forming the top electrode (TE) ion-supply layer and the counter inert bottom-electrode (BE) [2]. As induced by the applied field, the resulting oxidized Cu ions migrate through an insulating layer, reduce on the BE, and generate a conductive filament (CF) accounting for a change of resistance. Hence, insulating materials such as chalcogenides (Ag_2S and GeS) and oxides (Ta_2O_5) have been appropriately used to control the motion of Cu ions for ultralow-power computing systems and programmable logic applications, respectively [3], [4].

In this regard, we previously demonstrated a high-performance CBRAM device using an Al_2O_3 insulating layer [5], [6]. Due to the stability [5] and small size [7] of Cu in the Al_2O_3 matrix, a thermally stable and low-variability CBRAM device was successfully achieved [6].

On the other hand, we showed in [8] that the CF constriction is located closer to the W bottom electrode in this stack. Depending on the nature of the BE\oxide interface, the shape of the CF may change between conical and hourglass (HG), which in turn changes the CF constriction characteristics and thus the switching properties [8]. Various approaches aiming at controlling the formation of a HG-shaped CF were adopted. For example it was shown to be obtained using a specific programming scheme, which resulted in improved endurance properties [9]. This approach however implies that the application of a bias should be carefully adjusted by considering the trade-off between the cycling endurance and the memory window [10].

Therefore, rather than a programming bias scheme approach, a material stack engineering approach appears more appropriate to avoid trade-offs. In this work we introduce a WO_3 layer, serving as a good ionic conductor, in order to (i) strengthen the stability of the HG-shaped CF, thus (ii) improve the switching control of a resulting $\text{W}\backslash\text{WO}_3\backslash\text{Al}_2\text{O}_3\backslash\text{TiW}\backslash\text{Cu}$ CBRAM cell, and finally (iii) increase the memory state breakdown voltage, allowing reaching larger memory window.

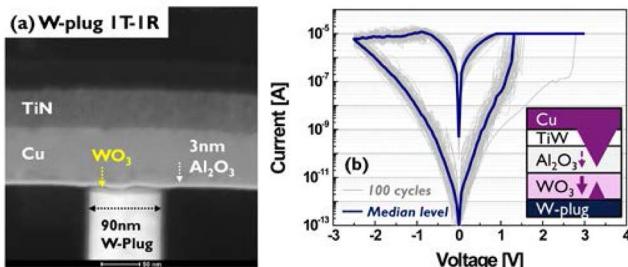


FIGURE 1. (a) Cross-sectional TEM image of the 1T1R CBRAM system on a 90-nm W plug. (b) Typical I-V characteristics of the $\text{W}\backslash\text{WO}_3\backslash\text{Al}_2\text{O}_3\backslash\text{TiW}\backslash\text{Cu}$ CBRAM device, where the gray lines are the traces of 100 cycles, and the bold line is the median level; note that the forming and switching loops are similar irrespective of the W oxidation temperature (400°C or 500°C); inset shows the filament growth.

II. EXPERIMENTS

The $\text{W}\backslash\text{WO}_3\backslash\text{Al}_2\text{O}_3\backslash\text{TiW}\backslash\text{Cu}$ CBRAM device is directly integrated on top of the drain side of a select-transistor in a 1-transistor/1-resistor scheme (1T1R). The detailed process flow is described in [6]. The 90nm-wide W-plug BE is submitted to a thermal oxidation process in order to form the WO_3 layer, as shown in Fig. 1(a). Then a 3nm-thick Al_2O_3 layer is deposited at 300°C using a H_2O -based atomic-layer deposition (ALD) technique. Prior to the deposition of the Cu-supply layer, the TiW layer is inserted to limit the indiffusion of Cu into the $\text{WO}_3\backslash\text{Al}_2\text{O}_3$ electrolyte stack during the passivation process.

III. RESULTS AND DISCUSSION

The switching current is fixed at $10 \mu\text{A}$ for low-power operation by controlling the word-line voltage during the forming and set processes. The set and reset operations can be achieved by applying a positive (negative) bias to the bit-line for the set (reset) operation. Fig. 1(b) shows the I-V characteristics of the fabricated 1T1R CBRAM device with the forming process at 3 V. A notably higher on/off ratio of more than 10^4 (read at -0.1 V) is obtained with a deeper high-resistance state (HRS) in the low-operating-current regime. The excellent device properties might be associated with the HG shape of the CF in $\text{WO}_3\backslash\text{Al}_2\text{O}_3$ bilayer system. When we consider the working principle of CBRAM, the formation of the Cu CF is governed by the predominant dynamic behavior between the electrochemical reaction and the ionic mobility of Cu ions in the material system [11]. That is, the state of the Cu ions in Al_2O_3 can be maintained as thermodynamically stable, and this result represents a relatively low ion conductivity [12]. On the other hand, a higher Cu mobility can be expected in WO_3 due to its well-known ionic conduction properties [13]. Hence, a realistic forming scenario is that a large number of Cu ions migrating from the Cu-source TE nucleates within the Al_2O_3 bulk (as described in [8]) because of the relatively slow ion movement. Then, the CF growth proceeds by successive local oxidation and reduction mechanisms of a protruding Cu virtual anode up to the WO_3 layer. When reaching the high ionic mobility WO_3

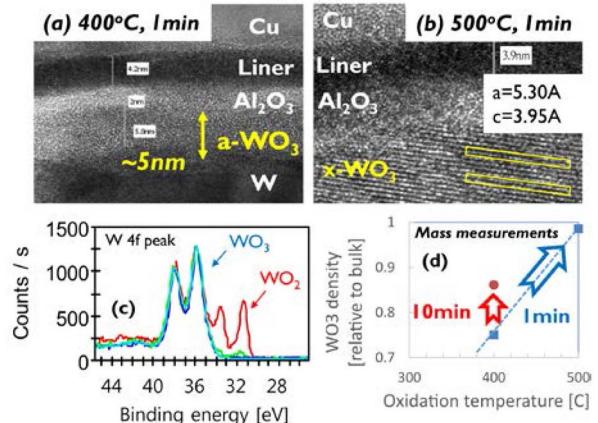


FIGURE 2. TEM images showing that the WO_3 phase changes from amorphous to tetragonal from (a) $T_{\text{ox}} = 400^\circ\text{C}$ to (b) $T_{\text{ox}} = 500^\circ\text{C}$. (c) X-Ray Photoemission Spectroscopy characterization showing that 10s short oxidation time at 400°C (red curve) results in mixed $\text{WO}_2\backslash\text{WO}_3$ stack whereas > 1min-long oxidation succeeds to form a single WO_3 phase. (d) Density calculations of the WO_3 layers extracted from mass measurements, evidencing strong densification from $T_{\text{ox}} = 400^\circ\text{C}$ to $T_{\text{ox}} = 500^\circ\text{C}$.

layer, the Cu ions supplied by this virtual Cu TE migrate fast toward the cathode without nucleation process, leading to the Cu plating on the cathode followed by the growth of an inverted cone-shaped Cu CF in WO_3 , as sketched in the inset of Fig. 1(b). Therefore, a HG-shaped CF with a constriction located closer to the $\text{WO}_3\backslash\text{Al}_2\text{O}_3$ interfaces can be achieved. The observed progressive reset behavior in the I-V trace further supports the explanation of the HG-shaped CF, which was confirmed by a conductive atomic force microscopy (C-AFM) study [8].

To understand the role of the introduced WO_3 layer with respect to the memory properties, a detailed physical investigation was performed by controlling several factors such as the oxidation temperature (T_{ox}) and time. As shown in Fig. 2(a), transmission electron microscopy (TEM) images revealed that an amorphous oxide (a- WO_3) was formed after 1 min of oxidation at $T_{\text{ox}} = 400^\circ\text{C}$. In contrast, Fig. 2(b) shows that a crystalline tetragonal oxide (x- WO_3) is formed when T_{ox} is increased to 500°C . Although both a- WO_3 and x- WO_3 layers were formed at different temperatures, X-Ray Photoemission Spectroscopy (XPS) revealed the same nature of chemical bonding, corresponding to WO_3 . On the other hand, Fig. 2(c) shows that shorter oxidation time at 400°C results in both WO_3 and WO_2 XPS peaks, indicating nonstoichiometric properties. Hence, forming a stoichiometric WO_3 layer requires at least 1min-long oxidation while the crystalline phase is controlled by the oxidation temperature of 500°C . Fig. 2(d) also shows that the layer density increases drastically from the amorphous microstructure obtained at 400°C to the crystalline phase obtained at 500°C .

Although the introduction of a WO_3 layer shows no impact on the set process, we observed that the oxidation

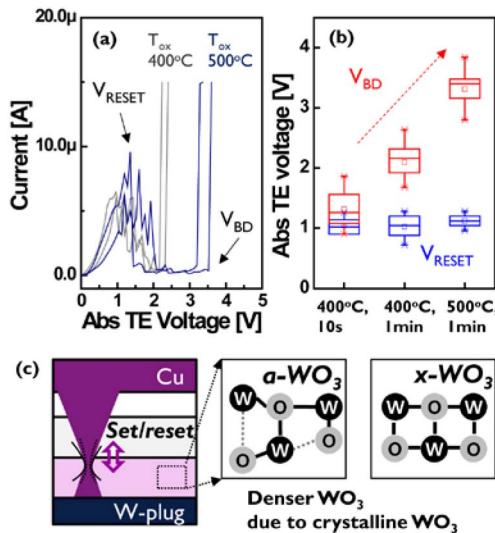


FIGURE 3. (a) Reset voltage ramps, evidencing an increase in the HRS breakdown voltage (V_{BD-HRS}) with the increase in the W oxidation temperature in accordance with higher-quality WO_3 . (b) Different V_{RESET} and V_{BD-HRS} parameters extracted from the DC I-V curves as a function of the oxidation temperature and time. (c) Schematic depicting that the increase in V_{BD-HRS} may be explained by the stronger bonding in $x\text{-WO}_3$.

conditions strongly affect the breakdown voltage in the HRS (V_{BD-HRS}), as shown in Figs. 3(a) and 3(b). V_{BD-HRS} is very low for the O-deficient WO_2/WO_3 bilayer obtained after 10 s of oxidation at 400°C . However, it increases with both the oxidation time and oxidation temperature. Based on quantum-point-contact I-V modeling, which describes the state conduction in our stack (see [7]), the constriction size is similar for these different oxidation conditions, which means that a larger value of V_{BD-HRS} is not related to a longer constriction but to the crystalline quality of the WO_3 material surrounding the CF constriction. The stronger breakdown robustness obtained for the WO_3 layer grown at 500°C is attributed to the improved microstructure, as evidenced in Fig. 2. This is also in agreement with the numerous W-O bonds formed in crystalline WO_3 compared with the amorphous structure [14], as illustrated in Fig. 3(c).

Therefore, the improved HRS breakdown strength of the optimized $x\text{-WO}_3/\text{Al}_2\text{O}_3$ stack allows using a larger reset pulse, which is a well-known knob allowing obtaining larger memory window [6]. Fig. 4(a) shows that while the Write cycling stress using a moderate reset pulse of -2 V leads to breakdown occurrences for $T_{ox} = 400^{\circ}\text{C}$, this failure is successfully suppressed for the device oxidized at 500°C . It is clearly evident that the improved switching robustness is related to an enhanced breakdown strength. Finally, and very importantly, the breakdown immunity obtained for the device oxidized at 500°C allows the memory window ($\sim 10^3$) to be substantially enlarged by using a larger reset-pulse amplitude (-2.5 V) during AC operation, which is demonstrated in Fig. 4(b).

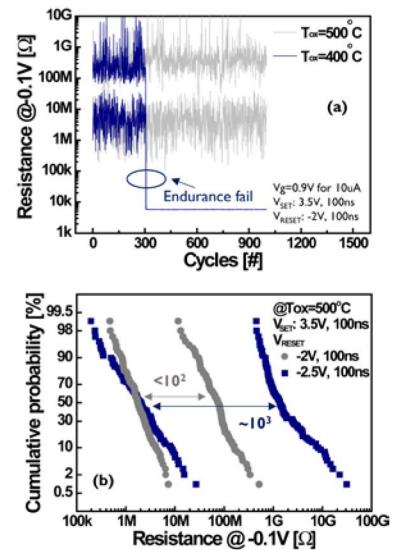


FIGURE 4. (a) Improved cycling robustness due to the suppressed breakdown failure for a device oxidized at 500°C . (b) The larger V_{BD-HRS} for $T_{ox} = 500^{\circ}\text{C}$ allows using larger reset-pulse amplitude (-2.5V), which in turn allows reaching larger memory window.

IV. CONCLUSION

We developed an $x\text{-WO}_3/\text{Al}_2\text{O}_3$ bilayer CBRAM device for low-current operation ($10\mu\text{A}$), which is desired for post-NAND applications. By introducing the ion-conductor WO_3 material by means of the thermal oxidation of the W plug, we optimized the control of the HG-shaped CF during switching. Furthermore, we demonstrated clear improvements of the microstructure and density of the WO_3 layer by increasing the oxidation time and temperature, resulting in a substantial increase of the HRS breakdown voltage. The optimized $x\text{-WO}_3/\text{Al}_2\text{O}_3$ bilayer CBRAM device allows for reliable cycling without breakdown and a larger memory window obtained using a larger reset pulse amplitude.

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AUGUSTO REDOLFI received the M.Sc. and Ph.D. degrees in electrical engineering from the University of Campinas, Campinas, Brazil.

He is currently with imec, Belgium, researching on process integration of resistive memories.



HYUNSANG HWANG received the Ph.D. degree in materials science from the University of Texas at Austin, Austin, TX, USA, in 1992.

He was with LG Semiconductor Corporation, Morristown, NJ, USA. He became a Professor of Materials Science and Engineering with the Gwangju Institute of Science and Technology, Gwangju, Korea, in 1997. In 2012, he moved to the Department of Materials Science and Engineering, Pohang University of Science and Technology, Korea.



MALGORZATA JURCZAK received the M.Sc. and Ph.D. degrees in electrical engineering from the Warsaw University of Technology, Warsaw, Poland.

She has been the Director of IMEC Emerging Memories Program, since 2011, focusing on resistive RAM memories.



LUDOVIC GOUX received the Ph.D. degree in engineering science from the University of Tours, France, in 2002. He is currently the Leader of the Memory Device Design Group, imec, Leuven, Belgium.



JIYONG WOO received the M.S. degree in materials science and engineering from the Gwangju Institute of Science and Technology, Gwangju, Korea, in 2012. He is currently pursuing the Ph.D. degree with the Department of Materials Science and Engineering, Pohang University of Science and Technology, Pohang, Korea.

He was an International Scholar with the Interuniversity Microelectronics Center, Leuven, Belgium, in 2015.



ATTILIO BELMONTE received the M.S. degree (Hons.) in electronic engineering from the Università della Calabria, Rende, Italy, in 2011. He is currently pursuing the Ph.D. degree in physics with the Interuniversity Microelectronics Center, Leuven, Belgium, and the Katholieke Universiteit Leuven.

He was a Visiting Scholar with the School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, USA, in 2015.