Received 18 June 2018; revised 13 August 2018; accepted 15 August 2018. Date of publication 17 August 2018; date of current version 27 August 2018.
The review of this paper was arranged by Editor C. Bulucea.

Digital Object Identifier 10.1109/JEDS.2018.2866026

Systematic DC/AC Performance Benchmarking of Sub-7-nm Node FinFETs and Nanosheet FETs

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This work was supported in part by the Ministry of Trade, Industry and Energy under Grant 10080617, in part by the Korea Semiconductor Research Consortium Support Program for the Development of the Future Semiconductor Device, in part by the National Research Foundation of Korea grant funded by the Ministry of Science, ICT under Grant NRF-2017R1C1B5017795, and in part by IC Design Education Center.

ABSTRACT In this paper, we systematically evaluate dc/ac performances of sub-7-nm node fin field-effect transistors (FinFETs) and nanosheet FETs (NSFETs) using fully calibrated 3-D TCAD. The stress effects of all the devices were carefully considered in terms of carrier mobility and velocity averaged within the active regions. For detailed AC analysis, the parasitic capacitances were extracted and decomposed into several components using TCAD RF simulation platform. FinFETs improved the gate electrostatics by decreasing fin widths to 5 nm, but the fin heights were unable to improve *RC* delay due to the trade-off between on-state currents and gate capacitances. The NSFETs have better on-state currents than do the FinFETs because of larger effective widths (W_{eff}) under the same device area. Particularly p-type NSFETs have larger compressive stress within the active regions affected by metal gate encircling all around the channels, thus improving carrier mobility and velocity much. On the other hand, the NSFETs have larger gate capacitances because larger W_{eff} increase the gate-to-source/drain overlap and outer-fringing capacitances. In spite of that, sub-7-nm node NSFETs attain better *RC* delay than sub-7-nm node as well as 10-nm node FinFETs for standard and high performance applications, showing better chance for scaling down to sub-7-nm node and beyond.

INDEX TERMS FinFET, NSFET, RC delay, stress effect, carrier mobility, parasitic capacitance, sub-7-nm node, DC/AC, benchmark.

I. INTRODUCTION

Silicon fin field-effect transistors (FinFETs) have been scaled down to 10-nm node by increasing fin height/width aspect ratio, adopting self-aligned diffusion/gate contacts, and removing dummy gate [1]. Several process advancements such as the higher aspect ratio, air-gap spacer, and lower resistive metals can also work as driving forces to scale down FinFETs [2]. However, it is highly challenging to scale down the physical device size in the following technology node while mitigating the short channel effects (SCEs) [3].

Meanwhile, nanosheet field-effect transistors (NSFETs) have been introduced by attaining superior gate electrostatics and better current drivability under the same device area [4], [5]. In addition, the NSFETs allow more degree of freedom for circuit design because NS widths are easily tuned, different from the quantized fins for FinFETs [6]. For appropriate device design guideline, however, it is important to evaluate DC/AC performances between FinFETs and NSFETs in sub-7-nm node considering several technical difficulties such as source/drain (S/D) junction gradients, stress effects, and middle-of-line (MOL) levels.

In this work, DC/AC performances of sub-7-nm node FinFETs and NSFETs were investigated for low power (LP), standard performance (SP), and high performance (HP) applications based on fully-calibrated TCAD platform. The performance metrics such as carrier mobility, velocity, and parasitic capacitance (C_{para}) components were also analyzed

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along with the stress effects to understand the physical origin of the DC and AC performances.

II. DEVICE STRUCTURE AND SIMULATION METHODOLOGY

Sub-7-nm node 2-fin FinFETs and 3-stacked NSFETs were simulated using Sentaurus TCAD [7]. Drift-diffusion transport equations, Poisson, and carrier continuity equations were calculated self-consistently. Slotboom bandgap narrowing model was included for all the Si and SiGe regions. Lombardi model for remote phonon and Coulomb scatterings, inversion and accumulation layer model for impurity, phonon, and surface roughness scatterings, and thin-layer model for the structural confinement of carriers were considered. Low-field ballistic mobility model was adopted to include quasi-ballistic effects. Shockley-Read-Hall, Auger, and Hurkx band-to-band tunneling recombination models were used. Stress-induced changes in band structure, effective mass, and effective density-of-states were also considered by deformation potential theory with two-band k·p model for electrons and six-band k·p model for holes.

Fig. 1 shows the schematic diagrams of 2-fin FinFETs (left) and NSFETs (right) targeting sub-7-nm node. The gate-last flow used in process simulation for FinFETs (black only) and NSFETs (black and red) was written at the right of Fig. 1a. Si/$Si_{0.7}Ge_{0.3}$ multi-layer deposition, inner-spacer formation, and $Si_{0.7}Ge_{0.3}$ removal for metal gate were also done as in [4]. The MOL was also considered for accurate performance evaluation by including cobalt metal-lines (M0) for gate, source, and drain contacts.

All the geometrical parameters are shown in Table 1. Channel and punch-through stopping regions were doped with boron (phosphorus) at 10^{15} and 2×10^{18} cm^{-3}, respectively, for n-type (p-type) devices. S/D regions for n-type (p-type) were doped with phosphorus (boron) at 10^{20} (5×10^{20}) cm^{-3}. Doping concentrations, S/D junction gradients, and physical parameters such as minimum low-field mobility, ballistic coefficients, saturation velocity, and quantum confinement of inversion charge were calibrated to the 10-nm node FinFETs [1], as shown in [8, Fig. 2]. Dielectric constants of IL, HK, and low-k regions were fixed at 3.9, 22, and 5.0, respectively, and the operation voltage (V_{DD}) is equal to 0.7 V. Parasitic contact resistances are fixed to 50 $\Omega\cdot\mu$m for each S/D regions. To make the device area (FP×CPP) of FinFETs and NSFETs equal, 2-fin FinFETs are compared to 3-stacked NSFETs (Fig. 1).

Several regions of the device generated during the process work as stressors for performance enhancement. Shallow Trench Isolation (STI) and M0 have a 1 GPa of tensile stress. TiN and work-function metal (WFM) have a 1 GPa of compressive (tensile) stress for n-type (p-type) devices. S/D regions have 2 % of C (50 % of Ge) for n-type (p-type) devices, which induce the internal stress at the active regions.

For the detailed analysis, C_{para} components of the devices are extracted using TCAD RF simulation platform (Fig. 2), modified from [9] and [10]. Gate terminal is node 1, drain terminal is node 2, and source and substrate terminals are grounded. Using the equivalent circuit of MOSFET ([11, Fig. 3]) in three different steps in Fig. 2 and Y parameters at different frequencies from 0.5 to 40 GHz, all the C_{para} components can be extracted at off-state. The C_{para} components were junction capacitances (C_{js}, C_{jd}) between S/D and

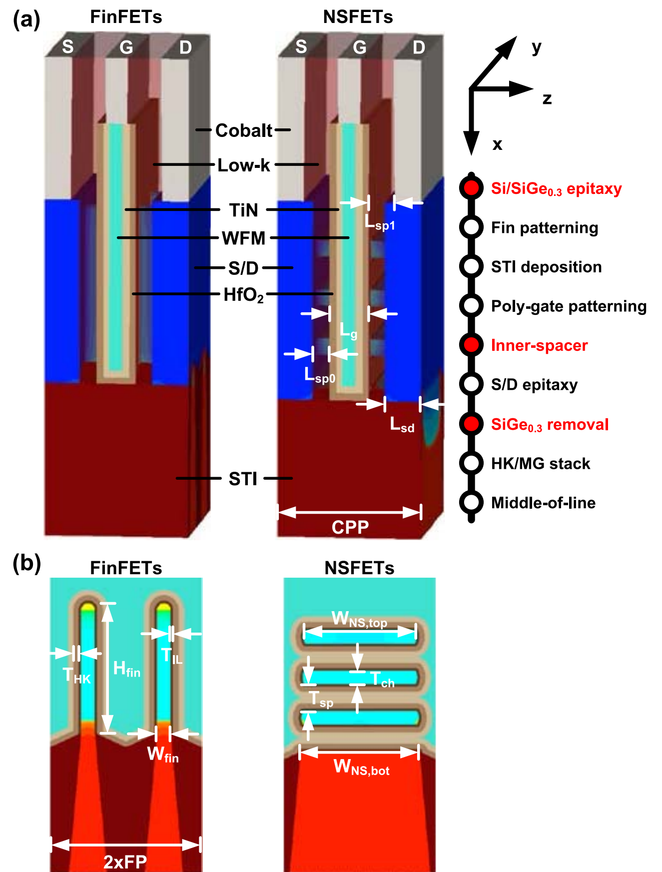

FIGURE 1. (a) Schematic diagrams of 2-fin FinFETs (left) and 3-stacked NSFETs (right), and (b) their cross-sections at the middle of channels specifying all the materials and geometrical parameters. The coordinate systems in 3D and process flows of the FinFETs (black only) and the NSFETs (black and red) are specified to the upper-right.

TABLE 1. Geometrical Parameters for Sub-7-nm Node FinFETs and NSFETs.

Devices	Geometrical Parameters		Values (nm)
Both	FP	Fin pitch	28
	CPP	Contacted poly (gate) pitch	44
	L_g	Gate length	12
	L_{sp0}	Spacer length between S/D and MG	5
	L_{sp1}	Spacer length between M0 and MG	7
	L_{sd}	S/D length	11
	T_{IL}	Interfacial layer thickness	1
	T_{HK}	High-k thickness	2
FinFETs	W_{fin}	Fin width	5, 6
	H_{fin}	Fin height	42 ~ 52
NSFETs	$W_{NS,top}$	Top-side NS width	40
	$W_{NS,bot}$	Bottom-side NS width	44
	T_{ch}	NS thickness	5
	T_{sp}	NS spacing	10

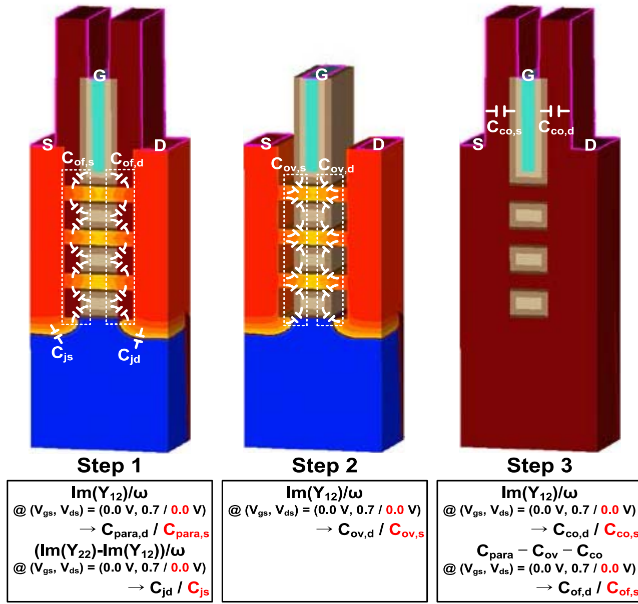

FIGURE 2. Detailed methods for the extraction of parasitic capacitances using TCAD RF simulation platform: junction capacitances (C_{js}, C_{jd}), overlap capacitances ($C_{ov,s}$, $C_{ov,d}$), contact capacitances ($C_{co,s}$, $C_{co,d}$), outer-fringing capacitances ($C_{of,s}$, $C_{of,d}$), and total parasitic capacitances ($C_{para,s}$, $C_{para,d}$).

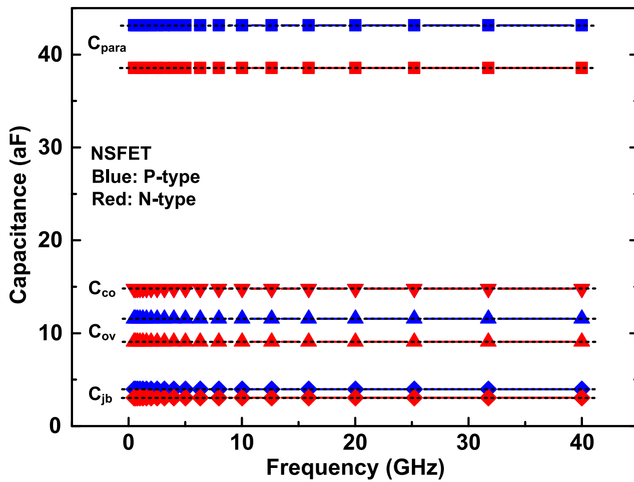

FIGURE 3. Extracted C_{para} components of the sub-7-nm node NSFETs at the drain-side. The extraction method is validated by showing constant C_{para} components as a function of frequency from 0.5 to 40 GHz.

substrate, overlap capacitances ($C_{ov,s}$, $C_{ov,d}$) between gate metal and S/D overlaps, contact capacitances ($C_{co,s}$, $C_{co,d}$) between M0 regions, and outer-fringing capacitances ($C_{of,s}$, $C_{of,d}$) between gate metal and S/D extension as well as S/D regions. It is validated that the C_{para} components are constant as a function of frequency, showing the fine extraction (Fig. 3).

III. RESULTS AND DISCUSSION

Fig. 4 shows the DC/AC performances of the 2-fin FinFETs having different W_{fin} and H_{fin} for SP applications (off-state current (I_{off}) is equal to 0.1 nA). The RC delay is calculated as $C_{gg}V_{DD}/I_{on}$, where C_{gg} is gate capacitance and I_{on} is on-state current at $V_{gs} = V_{ds} = V_{DD}$. N-type FinFETs show better DC/AC performances than p-type ones because the 10-nm node p-type FinFETs used for calibration have worse SCEs [1]. Both p- and n-type FinFETs with the W_{fin} of 5 nm have better I_{on} due to the reduction of SCEs. Usually, although higher H_{fin} have larger C_{gg} at on-state due to the increased inversion capacitance (C_{inv}), much improved I_{on} decreased the RC delay [10]. However, the sub-7-nm node FinFETs have almost similar RC delay for all different H_{fin} because larger C_{gg} increase offsets the DC performance (I_{on}) improvement. In other words, it does not bring any improvements in RC delay of the sub-7-nm node FinFETs by structural refinements of fins. It is essential to satisfy the W_{fin} of 5 nm or below for scaling the devices further, but it increases the process complexity [12].

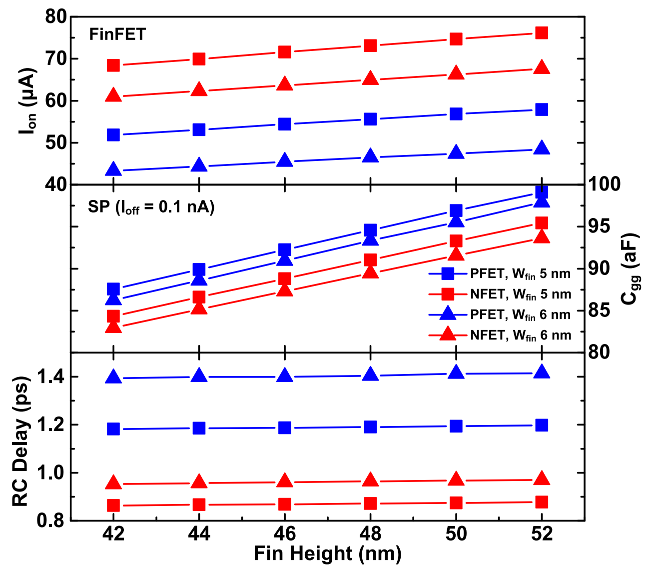

FIGURE 4. On-state currents (I_{on}), gate capacitances (C_{gg}), and RC delay of the sub-7-nm node FinFETs having different W_{fin} and H_{fin} for SP applications.

Fig. 5 shows the transfer characteristics and capacitances of the sub-7-nm node FinFETs (W_{fin} of 5 nm, H_{fin} of 48 nm) and NSFETs. The I_{off} is fixed to 1 nA for HP applications. The subthreshold swing (SS) and the drain-induced barrier lowering (DIBL) are almost the same between FinFETs and NSFETs, but the drain currents (I_{ds}) of the NSFETs near on-state are much greater than those of the FinFETs. However, the NSFETs have worse capacitance characteristics by showing larger C_{para} near off-state (Fig. 5b). P-type devices have larger C_{para} than do n-type devices because boron diffuses into the channel deeper than does phosphorus [3], [13].

Fig. 6 compares the I_{on} values of the sub-7-nm node FinFETs and NSFETs for all three applications (LP (I_{off} = 10 pA), SP, HP). The 10-nm node FinFETs (star symbols) are also included for comparison. It is clear that the sub-7-nm node FinFETs do not improve or even maintain the I_{on} of the

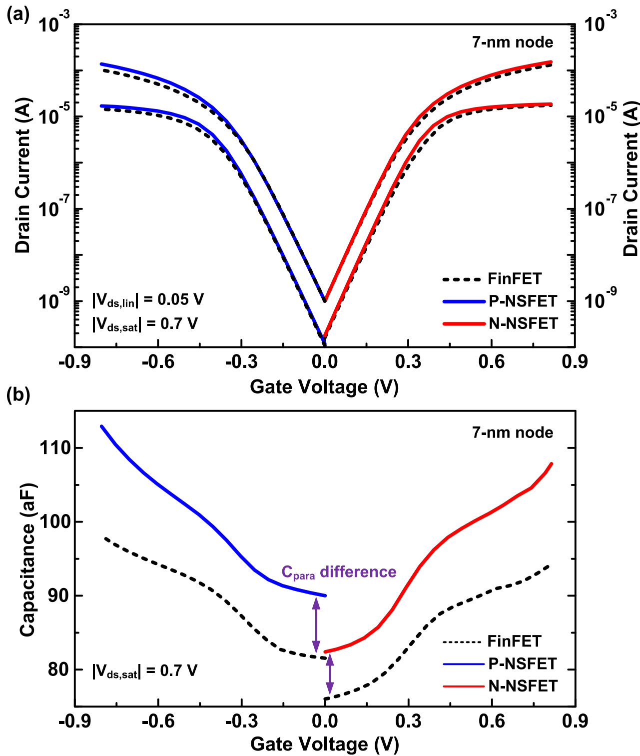

FIGURE 5. (a) Transfer characteristics and (b) capacitances of the sub-7-nm node FinFETs (dotted lines) and NSFETs (solid lines).

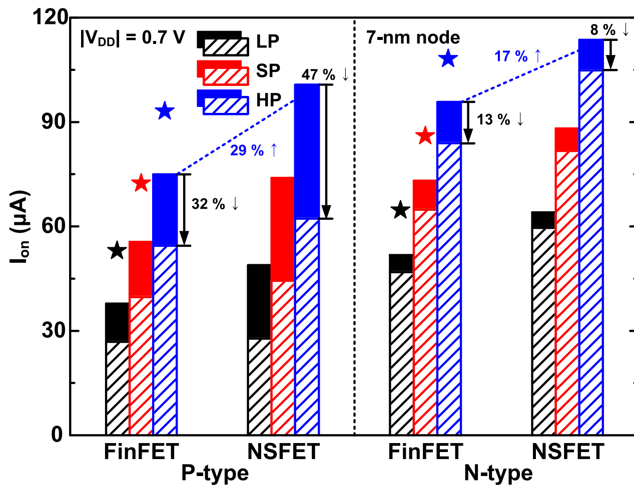

FIGURE 6. I_{on} values of the sub-7-nm node FinFETs and NSFETs with (solid) and without (shaded) stress effects for all three different applications. Star symbols represent the 10-nm node FinFETs with stress effects.

10-nm node FinFETs. DC performance of the FinFETs can be improved by increasing H_{fin} over 48 nm, but higher C_{gg} would cancel out the I_{on} improvement (Fig. 4). On the other hand, the sub-7-nm node NSFETs can improve the I_{on} for SP and HP applications because they have wider effective width (W_{eff}) inducing larger I_{ds} drivability under the same device area [5]; the W_{eff} for the NSFETs and the FinFETs are 282

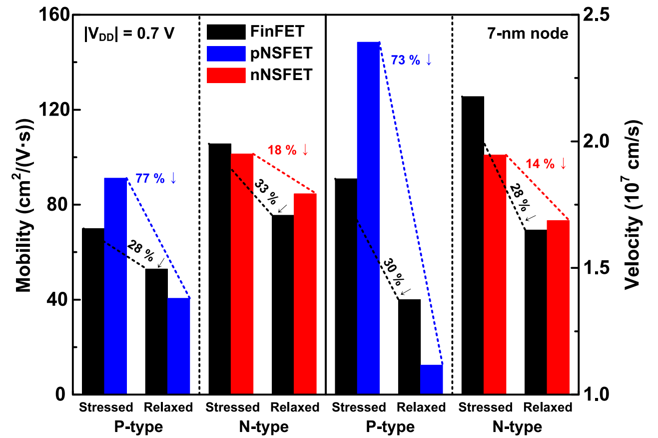

FIGURE 7. Carrier mobility and velocity of the sub-7-nm node FinFETs and NSFETs with and without stress effects.

TABLE 2. Stress Values of Sub-7-nm Node FinFETs and NSFETs.

Stress (GPa)	p-type FinFETs	p-type NSFETs	n-type FinFETs	n-type NSFETs
S_{xx}	1.47	-0.07	-0.64	0.04
S_{yy}	0.13	0.22	-0.14	0.27
S_{zz}	-2.29	-2.53	0.83	1.18

and 202 nm, respectively. The I_{on} values of the NSFETs for LP applications, however, are smaller than those of the 10-nm node FinFETs due to their degraded SCEs by S/D dopants diffusing into the channel.

Stress effects of the FinFETs and the NSFETs are also investigated by comparing between fully-stressed and fully-relaxed structures (Fig. 6). In HP application, for instance, both p- and n-type NSFETs have greater I_{on} than do FinFETs by 29 and 17 %, respectively. P-type devices have larger DC performance improvements by the stress than do n-type devices. Among all the devices, p-type NSFETs degrade the I_{on} most by 47 % for HP applications, whereas n-type NSFETs have the smallest I_{on} change of 8 % with and without stress.

These I_{on} changes can be clearly explained by the carrier mobility and velocity at on-state (Fig. 7). The NS channels have wide (100) surfaces but the fins have (110) sidewalls mostly. (100) electron and (110) hole mobility are larger than those at different surfaces [14], [15], thus hole mobility of FinFETs and electron mobility of NSFETs are larger for fully-relaxed devices. Both carrier mobility and velocity of p-type NSFETs are improved by the stress greatly, which brings about the I_{on} boosts significantly (Fig. 6). For fully-stressed ones, on the other hand, n-type NSFETs have worse carrier mobility and velocity than do n-type FinFETs.

To explain why the stress effects are different between FinFETs and NSFETs, average stress values within the active regions of the sub-7-nm node NSFETs and FinFETs are obtained in Table 2. Active region is defined as the channel regions within L_g controlled directly by gate. S_{xx}, S_{yy}, S_{zz}

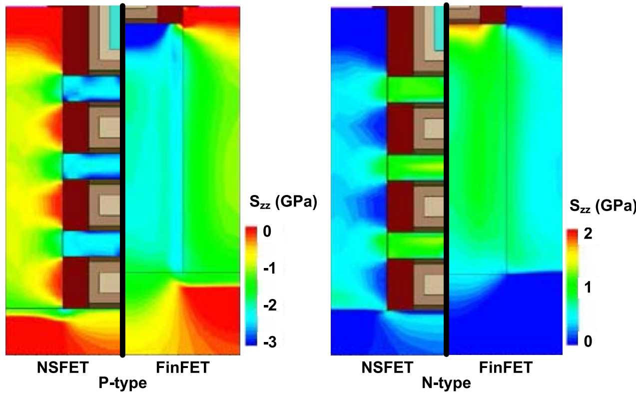

FIGURE 8. Stress profiles (S_{zz}) of the sub-7-nm node FinFETs and NSFETs.

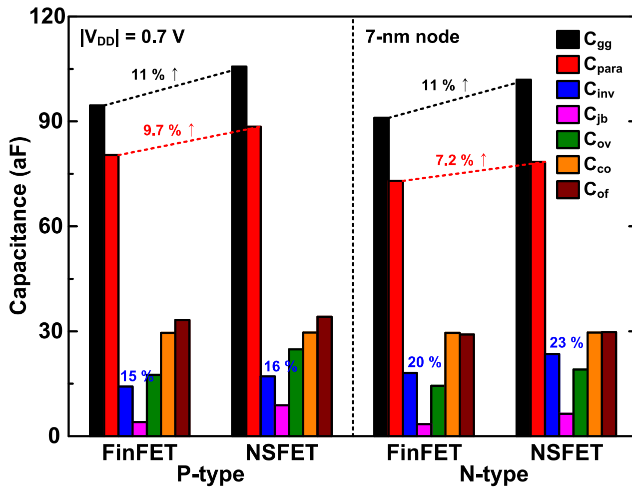

FIGURE 9. C_{gg}, C_{inv}, and C_{para} components of the sub-7-nm node FinFETs and NSFETs. The proportions of C_{inv} out of C_{gg} are also specified.

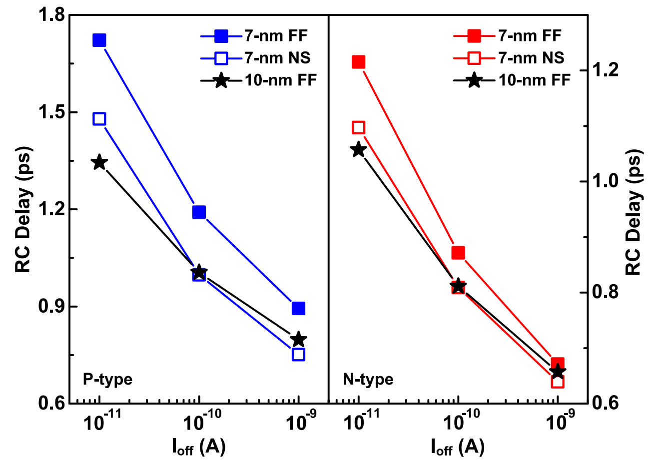

FIGURE 10. RC delay of the 10-nm node (star symbols), sub-7-nm node FinFETs (filled) and NSFETs (empty) for all different applications.

are stress components directing to the substrate, to the channel width, and to the gate length, respectively. Compressive stress is denoted as a negative sign in convenience for the directionality opposite to tensile stress.

P-type NSFETs have greater compressive stress of 2.53 GPa than do p-type FinFETs. P-type NSFETs have the metal gate encircling around the NS channels entirely, which holds the entire NS channels tightly and thus induces high compressive stress (the left of Fig. 8). N-type NSFETs also have this structural advantage to increase the tensile stress at the active channel regions (the right of Fig. 8). In the same manner, the metal gate of FinFETs holds top of the fins mostly where high S_{zz} are formed. About 0.2∼0.3 GPa tensile stress for the S_{yy} of NSFETs comes from the intermixed Ge and Si during $Si/Si_{0.7}Ge_{0.3}$ multi-layer epitaxy [16].

The reason for the small change of I_{on} by the stress for n-type NSFETs in Fig. 6 can be explained by the significant decrease of S_{xx}. Different from p-type devices, DC performance of n-type devices is improved by the tensile stress of S_{zz} as well as the compressive stress of S_{xx} [17]. Namely, narrow 5-nm-thick and three-stacked NS n-type channels lessen the compressive stress of S_{xx} induced by metal gate, thus reducing the stress effects to the I_{on}.

Fig. 9 shows the capacitances of the sub-7-nm node FinFETs and NSFETs. C_{para} components consider both source- and drain-side by adding each of them. C_{inv} values are obtained by subtracting C_{para} from C_{gg}. C_{gg} of the NSFETs are about 11 % larger than those of the FinFETs. Almost all the C_{para} components of the NSFETs are greater than those of the FinFETs due to the greater C_{ov} and C_{of} which are directly affected by the larger W_{eff}. Because the gate height at the MOL is kept constant, C_{co} values are same as 29.6 aF between the FinFETs and the NSFETs. P-type devices have larger C_{of} because of the larger S/D dopants diffusing into the channels. The NSFETs have larger C_{jb} due to their wider punch-through stopping regions. Comparing the proportions of C_{inv} out of C_{gg}, p-type devices are almost similar, whereas n-type NSFETs have the larger proportions of 23 % compared to n-type FinFETs. According as these, it is clarified that the greater I_{on} of n-type NSFETs than n-type FinFETs is not because of the carrier mobility and velocity in Fig. 7, but because of the current drivability by the wider W_{eff} indicated as larger C_{inv} in Fig. 9.

Fig. 10 summarizes the RC delay of the FinFETs and the NSFETs for all different applications. The sub-7-nm node FinFETs have larger RC delay in spite of smaller C_{gg} due to the critical decrease of I_{on}. The sub-7-nm node devices have larger RC delay for LP applications than the 10-nm node FinFETs because of worse SCEs, but the SCEs can be solved by increasing the channel doping with only a slight random dopant fluctuation [8]. Under the device scaling without additional technical process such as air-gap spacer and lower-resistive metal-lines [2], the sub-7-nm node NSFETs can outperform the 10-nm node FinFETs for SP and HP applications, thus showing the scalability down to sub-7-nm node and beyond.

IV. CONCLUSION

DC/AC performance evaluation targeting for the sub-7-nm node FinFETs and NSFETs was quantitatively analyzed through fully-calibrated TCAD simulations. The conventional design strategy of changing H_{fin} in the FinFETs is not advisable to reduce the RC delay due to the compensating effects between I_{on} and C_{gg}. Decreasing W_{fin}, instead, still boosts the I_{on} by improving the gate electrostatics, but increases the process complexity as a trade-off. The NSFETs show superior DC performance by increasing the current drivability through larger W_{eff} under the same footprint area compared to the FinFETs. Particularly, the p-type NSFETs increase the compressive stress of S_{zz} at the active region, which improves the carrier mobility and velocity at on-state, thus increasing the I_{on} greatly. The n-type NSFETs have greater I_{on} than do n-type FinFETs not because of the stress effects but because of larger W_{eff} increasing current drivability. Overall, the sub-7-nm node NSFETs show the great potential to scaling down as well as performance enhancement compared to the 10-nm node FinFETs for SP and HP applications.

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