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Flatband voltage control in p-metal gate metal-oxide-semiconductor field effect transistor by insertion of TiO_2 layer

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Titanium oxide (TiO_2) layer was used to control the flatband voltage (V_{FB}) of p-type metal-oxide-semiconductor field effect transistors. TiO_2 was deposited by plasma enhanced atomic layer deposition (PE-ALD) on hafnium oxide (HfO_2) gate dielectrics. Comparative studies between TiO_2 and Al_2O_3 as capping layer have shown that improved device properties with lower capacitance equivalent thickness (CET), interface state density (D_{it}), and flatband voltage (V_{FB}) shift were achieved by PE-ALD TiO_2 capping layer. © *2010 American Institute of Physics*. [doi:10.1063/1.3330929]

Among various high-k gate oxides, HfO_2 is a front up choice due to stable interface with silicon channel, preferable band offset, and good dielectric properties.[1] However, a large negative shift in the threshold voltage (V_{th}) up to 750 mV is a big concern for p-FETs.[1,2] The presence of positive fixed charges caused by oxygen vacancy (V_o) in HfO_2 was proposed to be a major cause for this phenomenon.[3] Since Al incorporation is supposed to compensate the V_o resulting in V_{th} shift, the use of Al_2O_3 or AlN capping layer or Al incorporation in gate oxides was proposed to suppress the V_{th} shift.[4–6] However, compared to rather well-established techniques for V_{th} shift control using capping or alloying the gate oxides with rare earth oxides for n-FET,[7,8] relatively little study has been reported for controlling V_{th} shift of p-FET.

Meanwhile, recent studies have shown that the SiO_2/high k interface plays a significant role in controlling V_{FB} shift due to dipole layer formation and vertical position of inserted layer is important for several different inserted oxide layers.[9,10] For n-FET, it was shown that the V_{th} tuning is strongly correlated with the electronegativity of rare earth element.[11] Thus, we expect that the insertion layer composed of elements with higher electronegativity than Hf in high-k/Si interface may increase the effective work function (EWF) for p-FETs. Finding additional element to tune the V_{FB} shift besides Al containing layer would be give us more degree of freedom in fabricating high performance metal-oxide-semiconductor field effect transistors (MOSFET) devices. In this article, we investigated the insertion of plasma enhanced atomic layer deposition (PE-ALD) TiO_2 layer for HfO_2 gate oxide for controlling the V_{FB} shift of p-FET and compared the electrical properties with Al_2O_3 insertion layer. TiO_2 was chosen due to the fact that Ti has the same electronegativity ($\cong$1.5) as Al but with relatively high dielectric constant.[1]

HfO_2 and TiO_2 layers were deposited by home-made PE-ALD system. For PE-ALD of TiO_2 and HfO_2 layers, tetrakis(dimethylamino)titanium and tetrakis(dimethylamino) hafnium were used as precursors, respectively, and oxygen plasma as a reactant. For PE-ALD La_2O_3 and Al_2O_3 layers, lanthanium(isopropyl)cyclopentadienyl [La(iPrCp)$_3$] and trimethylaluminium was used as La and Al precursors, respectively. The thicknesses of HfO_2 and each inserted layer were approximately 4 and 1 nm, respectively. The thickness was routinely measured using ellipsometry. X-ray photoelectron spectroscopy (XPS) measurements were carried out in Escalab 2201-XL equipped with a Mg K_α x-ray source and a hemispherical detector. Postdeposition annealing (PDA) and forming gas annealing (FGA) were carried out at 400 °C for 10 min in N_2 ambient and 400 °C for 30 min in H_2 5% $-N_2$ 95%, respectively. Ru was deposited using a dc magnetron sputtering as a metal gate through patterned shadow mask and Au was deposited using thermal evaporation as a backside electrode. Then, high temperature annealing (HTA) was performed at T_a=550, 700, and 800 °C for 10 s in vacuum to manifest the effect of Fermi level pinning (FLP) for each prepared sample. Capacitance-voltage (C-V) and current-voltage (I-V) characteristics were measured using Keithley 4200 semiconductor parameter analyzer and HP4284 LCR meter. The extraction of capacitance equivalent thickness (CET) values and interface state density (D_{it}) is described in our previous reports.[12,13]

Figure 1(a) shows XPS spectra in Al $2p$ binding energy region for as-deposited and HTA (T_a=800 °C) HfO_2 samples with Al_2O_3 top layer ($Si/HfO_2/Al_2O_3$). For both samples, Al $2p$ peak is observed clearly at 75 eV, indicating the presence of Al_2O_3 top layer. However, the intensity of this peak becomes smaller after HTA at 800 °C. Since XPS peak intensity is inversely proportional to the depth of atoms from the surface, we infer that the Al atoms diffused into the dielectric layer.[14] Similarly, Fig. 1(b) shows the XPS spectra of Ti $2p_{3/2}$ peak for as-deposited and HTA (T_a=800 °C) HfO_2 samples with TiO_2 top layer ($Si/HfO_2/TiO_2$). Similar to $Si/HfO_2/Al_2O_3$ sample, the intensity of Ti $2p_{3/2}$ peak at 460 eV decreased after HTA. Although we could not obtain depth profiles of Al or Ti due to its very small thickness ($\approx$4–5 nm), these results indicate that the HTA produces indiffusion of Al or Ti into the interface layer between high k and Si. Moreover, the deconvoluted XPS spectra in Fig. 1(b)

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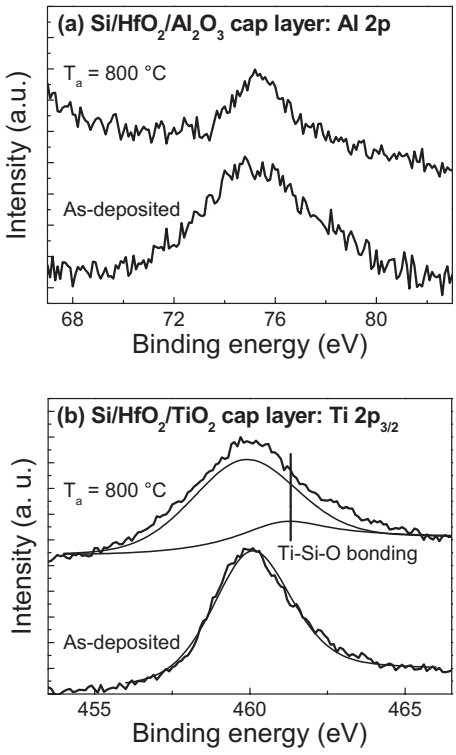

FIG. 1. XPS spectra for as-deposited and HTA (T_a=800 °C) HfO_2 samples with Al_2O_3 or TiO_2 capping layer: (a) Al $2p$ and (b) Ti $2p_{3/2}$.

shows the formation of Ti–Si–O bonding, clearly showing the indiffusion of Ti atoms to interface layer.

Figure 2(a) shows C-V curves for a MOS capacitor using HfO_2 as gate dielectric without any inserted layers after PDA and FGA, followed by HTA with varying T_a from 550 to 800 °C. The capacitance value decreases with increasing annealing temperature, due to the interfacial layer formation

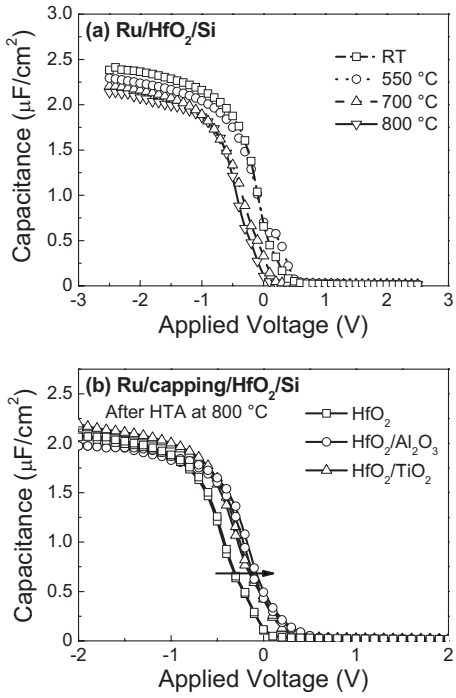

FIG. 2. (a) C-V curves of MOS capacitor with HfO_2 as a gate insulator after HTA from 550 to 800 °C (b) C-V curves of the MOS capacitors with HfO_2, HfO_2/Al_2O_3, and HfO_2/TiO_2 as a gate insulator after HTA at 800 °C.

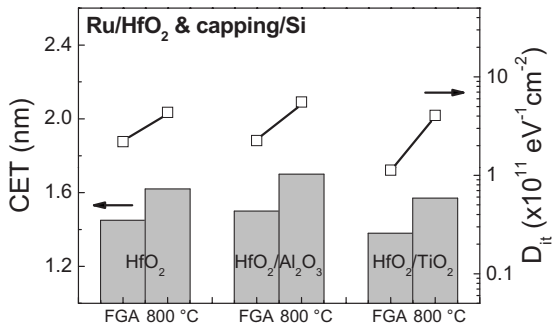

FIG. 3. CETs and D_{it} value of the MOS capacitors with HfO_2, HfO_2/Al_2O_3, and HfO_2/TiO_2 as a gate insulator after HTA at 800 °C.

at Si/HfO_2 interface. A shoulder is observed for the sample with T_a=550 °C, which is attributed to the formation of interface states originated from Hf diffusion and subsequent interfacial layer mixing.[15] Due to this, the V_{FB} was changed a little bit from 0.02 V to 0.24 eV after HTA at T_a =550 °C. However, after HTA at higher temperatures, the V_{FB} shifted to negative direction; −0.14 V at T_a=700 °C and −0.20 V at T_a=800 °C. Figure 2(b) shows C-V curves for Si/HfO_2 (no insertion layer), $Si/HfO_2/Al_2O_3$, and $Si/HfO_2/TiO_2$ samples after HTA at 800 °C. The MOS capacitors with Al_2O_3 and TiO_2 insertion layers have shown smaller V_{FB} shift (−0.15 and −0.12 eV, respectively) than that without any insertion layer (−0.22 eV), indicating that both Al_2O_3 and TiO_2 insertion layers effectively prevent the V_{th} shift for p-MOS capacitors after HTA process.

Figure 3 shows the CET and D_{it} values before and after HTA at 800 °C for these samples. For all these samples, the CET values increase after HTA, which is due to the formation of interface layer between HfO_2 and Si. Among the three samples, $Si/HfO_2/TiO_2$ has the smallest CET (1.38 and 1.57 nm before and after HTA), compared to the other (1.45 and 1.62 nm before and after HTA for pure HfO_2 and 1.50 and 1.70 nm before and after HTA for $Si/HfO_2/Al_2O_3$). This is primarily due to larger dielectric constant of TiO_2 (40–80) than that of Al_2O_3 (k=9) or HfO_2 (k=25).[1] Meanwhile, the D_{it} values were found to increase approximately twice after HTA for HfO_2 and $Si/HfO_2/Al_2O_3$. Before HTA, the D_{it} values of pure HfO_2 dielectric and Al_2O_3/HfO_2 are essentially identical ($\approx 2\times10^{11}$ eV^{-1} cm^{-2}), while that for $Si/HfO_2/TiO_2$ sample was smaller ($\approx 1\times10^{11}$ eV^{-1} cm^{-2}). This better D_{it} by using TiO_2 insertion layer agrees with a previous report.[16] These results clearly show that although the ability of tuning V_{FB} is almost same for Al_2O_3 and TiO_2 insertion layer, TiO_2 is a better choice due to the benefits in low CET and D_{it}.

Figure 4(a) shows C-V curves for MOS capacitors with HfO_2 gate oxide with top and bottom-inserted TiO_2 layer after HTA at 800 °C. There is only a mere difference in the capacitance depending on the position of inserted TiO_2 layer. However, we observe clear difference in V_{FB} depending on the position of inserted TiO_2 layer. Figure 4(b) shows δV_{FB} (δV_{FB}=V_{FB} of HfO_2/insertion layer—V_{FB} of HfO_2) for four different samples after HTA at 800 °C. Here, the top-inserted layers of Al_2O_3 and TiO_2 show similar values in terms of δV_{FB} (≈150 mV). However, larger δV_{FB} (≈250 mV) was achieved when TiO_2 is inserted at the bottom of HfO_2 layer. Thus, we infer that the high-k/Si interfacial layer plays a dominant role in tuning of V_{FB}. In other

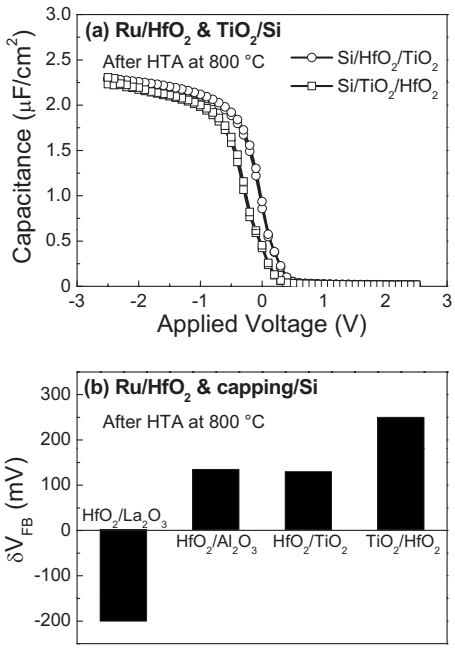

FIG. 4. (a) C-V curves of the MOS capacitors with HfO_2/TiO_2 and TiO_2/HfO_2 as a gate insulator (b) δV_{FB} of the MOS capacitors with HfO_2/La_2O_3, HfO_2/Al_2O_3, HfO_2/TiO_2, and TiO_2/HfO_2 as a gate insulator after HTA at 800 °C.

words, δV_{FB} is highly affected by the formation of an additional dipole layer at the HfO_2/Si interface. When Ti is located at the top of HfO_2, Ti atoms need to diffuse to high k/Si interface forming a dipole layer near the interface of the Si/HfO_2. Thus, the δV_{FB} is larger for bottom inserted TiO_2 layer compared to top-inserted TiO_2 layer. Finally, Fig. 4(b) also shows the result for La_2O_3 insertion layer to verify the polarity of V_{FB} shift, showing a negative shift V_{FB} ($\delta V_{FB} \approx -200$ mV) applicable in the n-FET device as reported previously.[7,8]

Based upon our current results with the findings in previous reports, we confirm that the primary cause for the V_{FB} tuning by inserted TiO_2 layer is an additional dipole layer formation at high-k/Si interfacial layer. The Ti atoms make Hf–O–Ti and Ti–O–Si configurations at the high-k/Si interface, generating dipole layers.[10,11] The strength and the direction of dipole vector depend on the electronegativity of the atoms, where the dipole strength has an inversely proportional relationship with electronegativity.[11] The electronegativity of Ti is approximately same as that of Al (1.5) which is larger than that of Hf (1.3), and smaller than that of Si (1.8).[17] Thus, the direction of dipole vector is determined toward to the Si substrate because the +Q pole is formed on both Hf and Ti in Hf–O–Ti and Ti–O–Si configurations, respectively. After the dipole formation, the EWF of metal gate increases due to effect of (+) electric field from the interface dipoles, minimizing the FLP effect.

In this study, systematical studies were conducted on the properties of TiO_2 insertion layer to increase the EWF, and thereby reduce the FLP effect in p-FETs. The results show that the HfO_2-based gate dielectric with inserted TiO_2 layer can move the V_{FB} into (+) direction after HTA process compared to the device that used only HfO_2 as gate oxide without any insertion layers. Considering the amount of V_{FB} shift and CET from the sample with TiO_2 layer inserted at the bottom of HfO_2 gate dielectric, TiO_2 insertion layer can be regarded as a highly promising candidate for suppression of FLP effect in p-FETs with HfO_2 gate dielectrics.

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