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Bottom Oxide Bulk FinFETs Without Punch-Through-Stopper for Extending Toward 5-nm Node

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ABSTRACT Structural advancements of 5-nm node bulk fin-shaped field-effect transistors (FinFETs) without punch-through-stopper (PTS) were introduced using fully calibrated TCAD for the first time. It is challenging to scale down conventional bulk FinFETs into 5-nm technology node due to the sub-fin leakage increase. Meanwhile, bottom oxide deposition after anisotropic etching for source/drain (S/D) epi formation prevents the sub-fin leakage effectively even without the PTS doping, thus achieving better gate-to-channel controllability. Bottom oxide FinFETs also have smaller gate capacitances than do conventional FinFETs because the parasitic capacitances decrease by smaller S/D epi separated from the bottom Si layer, which reduces junction and outer-fringing capacitances. But smaller S/D epi decreases the stresses along the channel direction, and the effective widths decrease by the bottom oxide layer blocking the current paths at the bottom side of fin channels. Furthermore, increase of the interconnect resistance and capacitance parasitics down to 5-nm node diminishes the improvements of total delays as the interconnect wire length increases greatly. In spite of these drawbacks, 5-nm node bottom oxide FinFETs achieve smaller total delays than do the 7-nm node conventional FinFETs, especially for low-power applications, thus promising for the scalability of bulk FinFETs along with simple and reliable process by avoiding PTS step.

INDEX TERMS 5-nm node, bottom oxide, FinFETs, punch-through-stopper (PTS), intrinsic delay, total delay, sub-fin leakage.

I. INTRODUCTION

Si fin-shaped field-effect transistors (FinFETs) have been scaled down from 14-nm node [1] to 10-nm node [2] by forming high-aspect-ratio fin and optimizing layouts to increase the device density. Much thinner fin is required to maintain good electrostatics in sub-10-nm node [3], but too-narrow fin widths (W_{fin}) below 4 nm induce lower carrier mobility and greater parasitic resistance [4].

Meanwhile, a heavy punch-through-stopper (PTS) doping is mandatory to block sub-fin leakage of the bulk FinFETs [1], [5]–[7]. However, PTS doping degrades carrier mobility within the fin channel [6] and induces performance variations by the PTS dopants [8]. Several efforts to reduce or eliminate PTS doping have been introduced. Bottom oxidation after sub-fin recess enables silicon-on-insulator-like FinFETs, but shows structural instability and induces the variations of fin height (H_{fin}) [9]. Quantum barrier is another method to reduce sub-fin leakage by bandgap engineering, but different material compositions between sub-fin and channel induce process complexity and variations in the position of quantum barrier [5].

Thus, in this work, a simple and feasible device structure to prevent sub-fin leakage without PTS doping is proposed. DC/AC performances of all the bulk and proposed FinFETs including front-end- as well as back-end-of-lines

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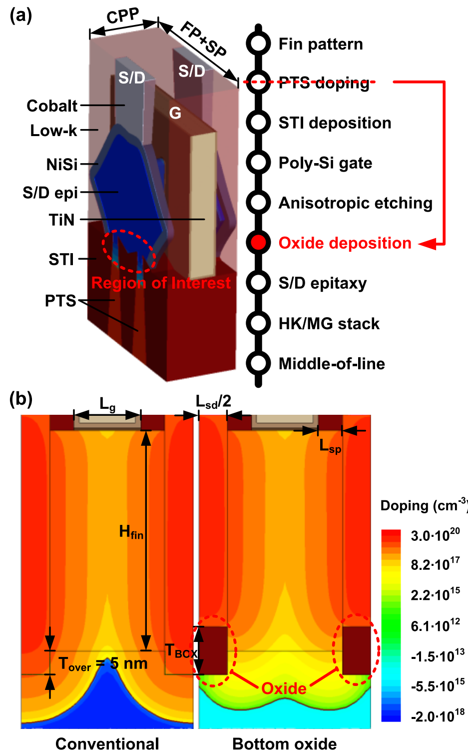

FIGURE 1. (a) 3-D schematic diagram and process flow of 2-fin bulk FinFETs and (b) 2-D cross-sections of the conventional and bottom oxide FinFETs. Region of interest and bottom oxide of the bulk FinFETs are specified as red.

are analyzed and compared in the different technology nodes down to 5-nm node.

II. DEVICE STRUCTURE AND SIMULATION METHOD

All the FinFETs were simulated using Sentaurus TCAD [10]. Drift-diffusion transport model was calculated self-consistently with Poisson and electron/hole continuity equations. Quantum confinements within the fin channels were considered by density-gradient model. Mobility, recombination, and deformation potential models were equivalent as in [11].

Fig. 1a shows a schematic diagram and process flow of the 2-fin bulk FinFETs. All the FinFETs have the diamond-shaped source/drain (S/D) epi over-etching the PTS layer by 5 nm, which is feasible and generally formed [1], [12], [13]. Contact resistivity at the NiSi interface wrapping all around the S/D epi is $5 \times 10^{-9} \Omega \cdot \text{cm}^2$. Conventional FinFETs adopt the PTS doping at 2×10^{18} cm^{-3} to prevent the sub-fin leakage, whereas the proposed bottom oxide FinFETs have the oxide layer deposited after anisotropic etching for S/D epi formation without the PTS doping (Fig. 1b). The bottom oxide thickness (T_{BOX}) was varied as 5, 10, 15 nm. Bottom oxide FinFETs have the oxide layer beneath the S/D epi only and the fin channel adjoining to the Si substrate, which possibly alleviates self-heating effects [14] that silicon-on-insulator FinFETs suffer mostly from.

TABLE 1. Geometrical parameters of the 2-fin Bulk FinFETs in advanced technology nodes.

Geometrical Parameters		Values (nm)		
		10-nm	7-nm	5-nm
CPP	Contacted poly-gate pitch	54	44	36
FP	Fin pitch	34	30	26
SP	P/N-type separation length	68	60	58
L_g	Gate length	18	16	14
L_{sp}	Spacer length	7	6	5
L_{sd}	S/D length	22	16	12
W_{fin}	Fin width	7	6	5
H_{fin}	Fin height	46	46	46

TABLE 2. Interconnect RC parasitics in advanced different technology nodes from [15].

Interconnect RC Parasitics		Technology Node		
		10-nm	7-nm	5-nm
R_{int}	Resistance (Ω/μm)	120	347	497
C_{int}	Capacitance (aF/μm)	260	271	314

All the TCAD results were calibrated to the 10-nm node FinFETs [2]. S/D doping profiles were tuned first to fit the subthreshold swing (SS) and drain-induced barrier lowering (DIBL). Ballistic coefficient and saturation velocity were then tuned by Monte Carlo simulation. Several mobility parameters related to surface roughness scattering were tuned to fit the drain currents (I_{ds}) in the inversion region. Table 1 defines the geometrical parameters of the FinFETs in advanced technology nodes. Equivalent oxide thickness of all the devices is 0.7 nm. The SP defines the separation length between n-type FETs (NFETs) and p-type FETs (PFETs). This parameter is not scalable below 58 nm because the large S/D epi is overlapped with adjacent transistors [15].

Table 2 shows the interconnect resistance and capacitance (RC) parasitics per unit wire length (L_{wire}) in three different technology nodes [15] to analyze front-end- as well as back-end-of-line delay components quantitatively. The L_{wire} was varied as 2 × CPP, 20 × CPP, and 100 × CPP for short, medium, and long interconnect wires, respectively.

III. RESULTS AND DISCUSSION

Fig. 2a shows the transfer characteristics of the conventional and bottom oxide bulk FinFETs at the operation voltage (V_{DD}) of 0.7 V. As the technology nodes decrease, sub-fin leakage of the conventional FinFETs increases. However, 5-nm node bottom oxide FinFETs maintain the small SS similar to the 10-nm node devices. The bottom oxide FinFETs also have smaller gate capacitances than do the conventional FinFETs (Fig. 2b). The gate capacitances decrease further as the T_{BOX} increases because the S/D epi becomes smaller by the oxide layer (the inset of Fig. 2b), thus decreasing outer-fringing capacitances [16]. The S/D epi is formed by crystallographic deposition having different deposition rates in each crystal directions of <100>, <110>, and <111> at the Si regions selectively [17]. The conventional FinFETs

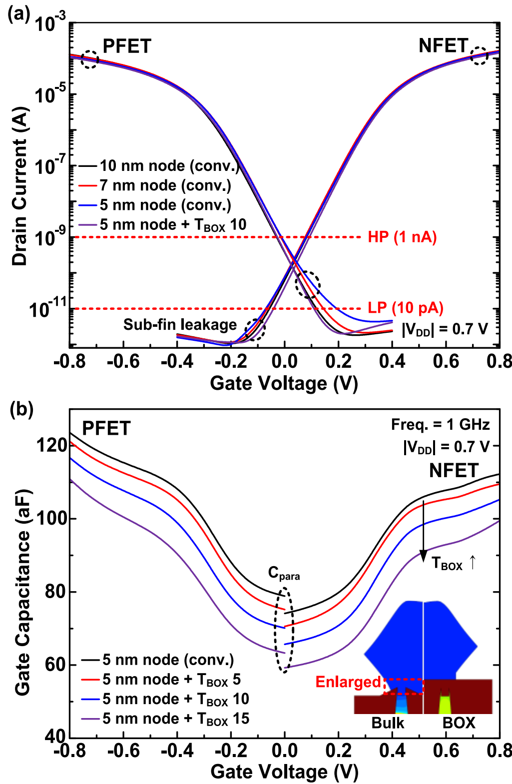

FIGURE 2. (a) Transfer characteristics of the FinFETs in different technology nodes and (b) gate capacitances of the 5-nm node FinFETs with different T_{BOX}.

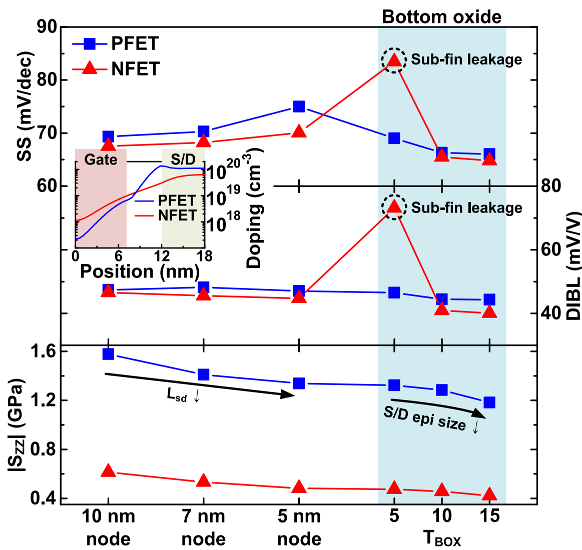

FIGURE 3. Short channel characteristics (SS, DIBL) and stresses along the channel direction (S_{ZZ}) of the FinFETs. Left inset shows the doping profiles of the bottom oxide FinFETs (T_{BOX} = 5 nm) obtained above the 1 nm of the bottom oxide layer at the middle of fin.

have larger Si area than the bottom oxide FinFETs because both fin and bottom regions are exposed. Thus, larger S/D epi is formed for the conventional devices under the same crystal growth time.

Fig. 3 shows SS, DIBL, and stresses along the channel direction (S_{ZZ}) of the FinFETs. SS and DIBL values are

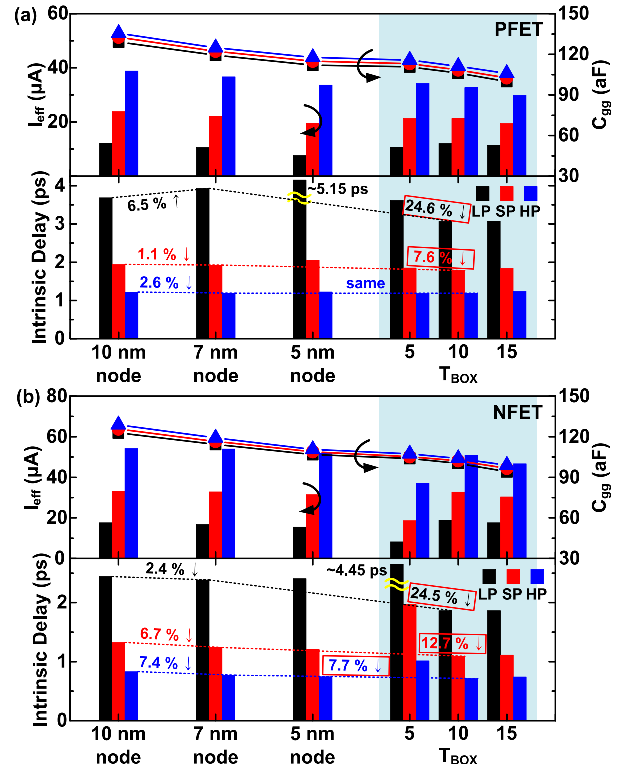

FIGURE 4. I_{on}, C_{gg}, and intrinsic delay of the FinFETs for LP (I_{off} = 10 pA), SP (I_{off} = 0.1 nA), and HP (I_{off} = 1 nA) applications.

extracted using the same method as in [18]. S_{ZZ} values are obtained by integrating all the active regions of the devices [11]. SS increases as the technology node decreases, but 5-nm node bottom oxide FinFETs decrease both SS and DIBL by achieving better gate-to-channel controllability. Too large SS and DIBL for the bottom oxide NFETs (T_{BOX} = 5 nm) without PTS are understood by the left inset of Fig. 3. The PFETs have smaller dopant penetrations into the gate region because the boron dopants in $Si_{0.5}Ge_{0.5}$ S/D epi of the PFETs are segregated by Ge [19] and reside mostly at the S/D extensions. High doping at the S/D extensions of the PFETs increases the parasitic capacitances (C_{para}) compared to the NFETs [20] as shown in Fig. 2b. The $|S_{ZZ}|$ of both P- and NFETs decrease as the S/D epi size decreases by the L_{sd} decrease from 10- to 5-nm node and by the T_{BOX} increase.

Fig. 4 shows DC/AC performances of all the FinFETs in front-end-of-line. On-state currents (I_{on}) and capacitances (C_{gg}) were extracted at the gate and drain voltages of V_{DD}, whereas effective currents (I_{eff}) and intrinsic delays were obtained from the eqs. 5 and 4 in [21], respectively, given by

$$I_{eff} = \frac{I_H - I_L}{\ln(I_H/I_L)} \tag{1}$$

$$intrinsic\ delay = \frac{C_{gg}V_{dd}}{2I_{eff}} \tag{2}$$

where off-state currents (I_{off}) are fixed at 10 pA, 0.1 nA, and 1 nA for low-power (LP), standard-performance (SP), and

TABLE 3. DC performance variations of 5-nm node FinFETs by random dopant fluctuation and work-function variation.

5-nm Technology Node HP application (I_{off}= 1 nA)		Conventional FinFET		Bottom Oxide FinFET	
		PFET	NFET	PFET	NFET
$\sigma V_{th}\,(mV)$	RDF	1.7	4.8	2.9	4.9
	WFV	11.4	10.5	12.3	11.1
$\sigma I_{on}/\langle I_{on}\rangle\,(\%)$	RDF	0.86	0.96	1.40	0.61
	WFV	2.81	2.85	2.84	2.78
$\sigma I_{off}\,(nA)$	RDF	0.85	0.53	0.40	0.43
	WFV	0.82	0.33	0.44	0.39

high-performance (HP) applications, respectively, by shifting the gate work function. Threshold voltages (V_{th}) were extracted using constant current method at 10^{-7} A.

For the PFETs, I_{eff} decreases from 10- to 5-nm node by smaller L_{sd} and larger SS (Fig. 4a). Continuous decrease of C_{gg} by the technology node scaling enables to the intrinsic delay decrease at 7-nm node, but not at 5-nm node due to the SS increase. 5-nm node bottom oxide PFETs, on the other hand, decrease the intrinsic delay for LP and SP applications by 24.6 % and 7.6 %, respectively, compared to the 7-nm node devices by decreasing C_{gg} and SS. For HP applications, intrinsic delay of the bottom oxide PFETs is not improved because smaller S_{ZZ} and effective width ($W_{eff} = W_{fin} + 2 \times H_{fin}$) by the bottom oxide layer decrease I_{eff} critically.

For the NFETs, intrinsic delay decreases from 10- to 7-nm node for all the applications. 5-nm node conventional NFETs suffer from the intrinsic delay increase for LP applications due to the SS increase. 5-nm node bottom oxide NFETs, however, decrease the intrinsic delays by 24.5 %, 12.7 %, and 7.7 % for LP, SP, and HP applications, respectively, compared to the 7-nm node devices.

For bottom oxide FinFETs, there is a trade-off between DC and AC performances with respect to T_{BOX}; the increase of T_{BOX} decreases the C_{gg}, but also decreases the S_{ZZ} and the W_{eff}. The bottom oxide FinFETs with T_{BOX} around 10 nm have smaller DC performances but much superior AC performances and electrostatics than do the conventional FinFETs.

Random dopant fluctuation (RDF) and work-function variation (WFV) effects on DC performance of the FinFETs are also analyzed through statistical impedance field method [22]. The number of randomized devices is 10,000 each for RDF and WFV. Phosphorus and boron dopants of the PTS layer for P- and NFETs were randomized only for the RDF study, whereas the WF was randomized as a number of 5-nm-size grains having different WF values of 4.6 and 4.4 eV for <200> and <111> orientations with probabilities of 60 and 40 %, respectively [23].

Table 3 shows the DC performance variations of conventional and bottom oxide FinFETs in the 5-nm node. I_{on} variations are calculated as the standard deviations divided by the averages because the I_{on} levels between P- and NFETs are different [24]. RDF induces small variations of V_{th} and I_{on} even for the conventional devices because little PTS

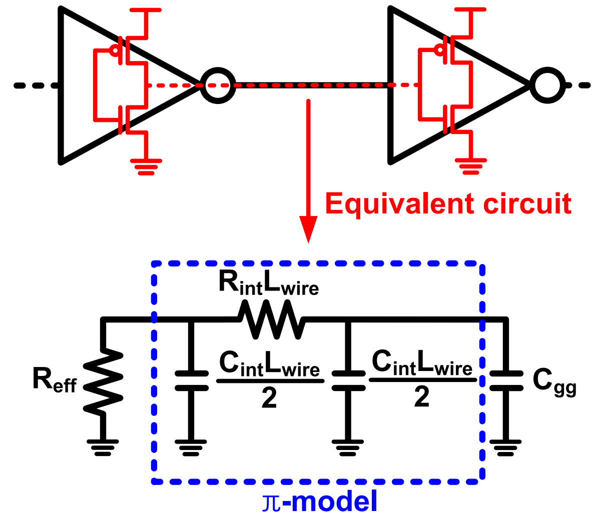

FIGURE 5. Schematic diagram of CMOS inverters connected in series (top) and equivalent circuit including interconnect RC parasitics (bottom).

dopants diffuse into the channels with the junction gradients of 4.2 and 4.4 nm/dec for P- and NFETs, respectively, similar to the super-steep retrograde devices [25]. WFV dominantly varies the DC performance, but both conventional and bottom oxide FinFETs have similar variations. However, the conventional PFETs have greater I_{off} variations by RDF or WFV because the sub-fin leakage increases critically for some of the devices whose bottom fins lose gate-to-channel controllability.

A series of CMOS inverters and its equivalent circuit are shown in Fig. 5 by considering the interconnect RC parasitics. Total delay was calculated using Elmore delay calculation and π-model for lumped RC interconnect model [26], represented by

$$\tau_{total} = C_{gg}R_{eff} + C_{int}R_{eff}L_{wire} + C_{gg}R_{int}L_{wire} + \frac{C_{int}R_{int}}{2}L_{wire}^2 \quad (3)$$

where R_{eff} is the effective resistance calculated as $V_{dd}/(2\times I_{eff})$. First term on the right side represents intrinsic delay, the next two terms are mixed between intrinsic and interconnect components, and the last term is from the interconnect RC parasitics only. In this work, total delays for each of the P- and NFETs are considered for simplicity.

Total delays of all the FinFETs for short (2 × CPP), medium (20 × CPP), and long (100 × CPP) L_{wire} for SP application are shown in Fig. 6. As the L_{wire} increases, the degree of improvements of the total delays is reduced from 6.4 % (11.3 %), 3.0 % (7.2 %), to 0.9 % (4.5 %) for PFETs (NFETs), respectively. Furthermore, even as the devices are scaled down from 7- to 5-nm node and the bottom oxides are used, the total delays for HP applications rather increase by 6.0 % and 0.9 % for PFETs and NFETs, respectively.

Most of the total delays are affected by intrinsic delays for short L_{wire}, whereas those are dominantly increased by interconnect RC parasitics for medium and long L_{wire}

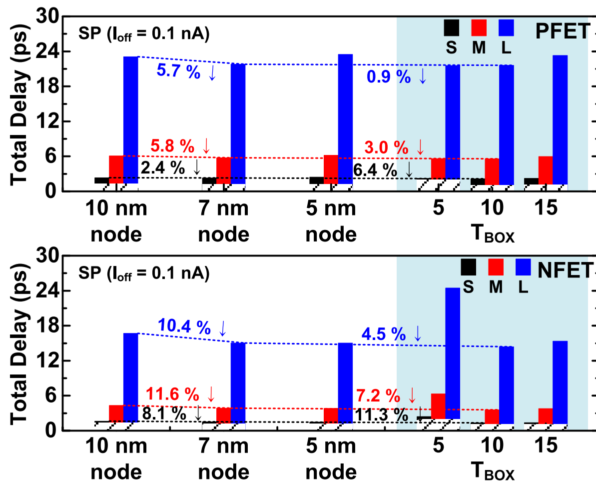

FIGURE 6. Total delay of all the FinFETs for short (2 × CPP), medium (20 × CPP), and long (100 × CPP) interconnect wire lengths for SP (I_{off} = 0.1 nA) application. Shaded bars represent the intrinsic delays of the devices.

(especially by $C_{int}R_{eff}L_{wire}$). Since the C_{int} increases greatly from 7- to 5-nm node rather than from 10- to 7-nm node, the improvements of the total delays from 7- to 5-nm node diminish with L_{wire}. This effect increases as the I_{eff} (inversely proportional to R_{eff}) is degraded, especially for HP application. But in spite of the interconnect RC parasitics, bottom oxide FinFETs can achieve the smallest total delays for LP and SP applications, feasible for the scalability of the bulk FinFETs down to the 5-nm node along with the process simplicity by avoiding the PTS doping.

IV. CONCLUSION

Superior performances of 5-nm node bottom oxide FinFETs were demonstrated using fully calibrated TCAD. The bottom oxide layer prevents the sub-fin leakage of the FinFETs effectively without the PTS doping, thus maintaining small SS and DIBL. Smaller S/D epi of the bottom oxide FinFETs also decreases the C_{para} and C_{gg}, thus improving intrinsic delays in the 5-nm node compared to the conventional FinFETs in previous technology nodes. The bottom oxide FinFETs are much immune to the RDF and WFV than the conventional devices by preventing the bottom fin layers which are vulnerable to the sub-fin leakages. Although the interconnect RC parasitics degrade the AC performances critically at 5-nm node, the bottom oxide FinFETs achieve the smallest total delays for all the L_{wire} cases for LP and SP applications. Therefore, bottom oxide structure is highly recommended to attain smaller total delay, simpler and much reliable process by skipping the PTS step.

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